

COMPAL CONFIDENTIAL

MODEL NAME : Loki-G 15/17
MB PCB PN : DAA000FC010
PWR/B PCB PN : DA4002L3010
IO/B PCB PN : DA6001XF010

ZZZ

PCB R1

DAA000FC010

PCB@

UC1

CPU R1

SA0000BPJ1L

I5@

UC1

SA0000BPZ1L

I7@

UC1

CPU R3

SA0000BPJ2L

I5@

UC1

SA0000BPZ2L


I7@

Dell/Compal Confidential
Schematic Document

COFFEE LAKE H
N17P-G0/G1
Loki-G 15/17

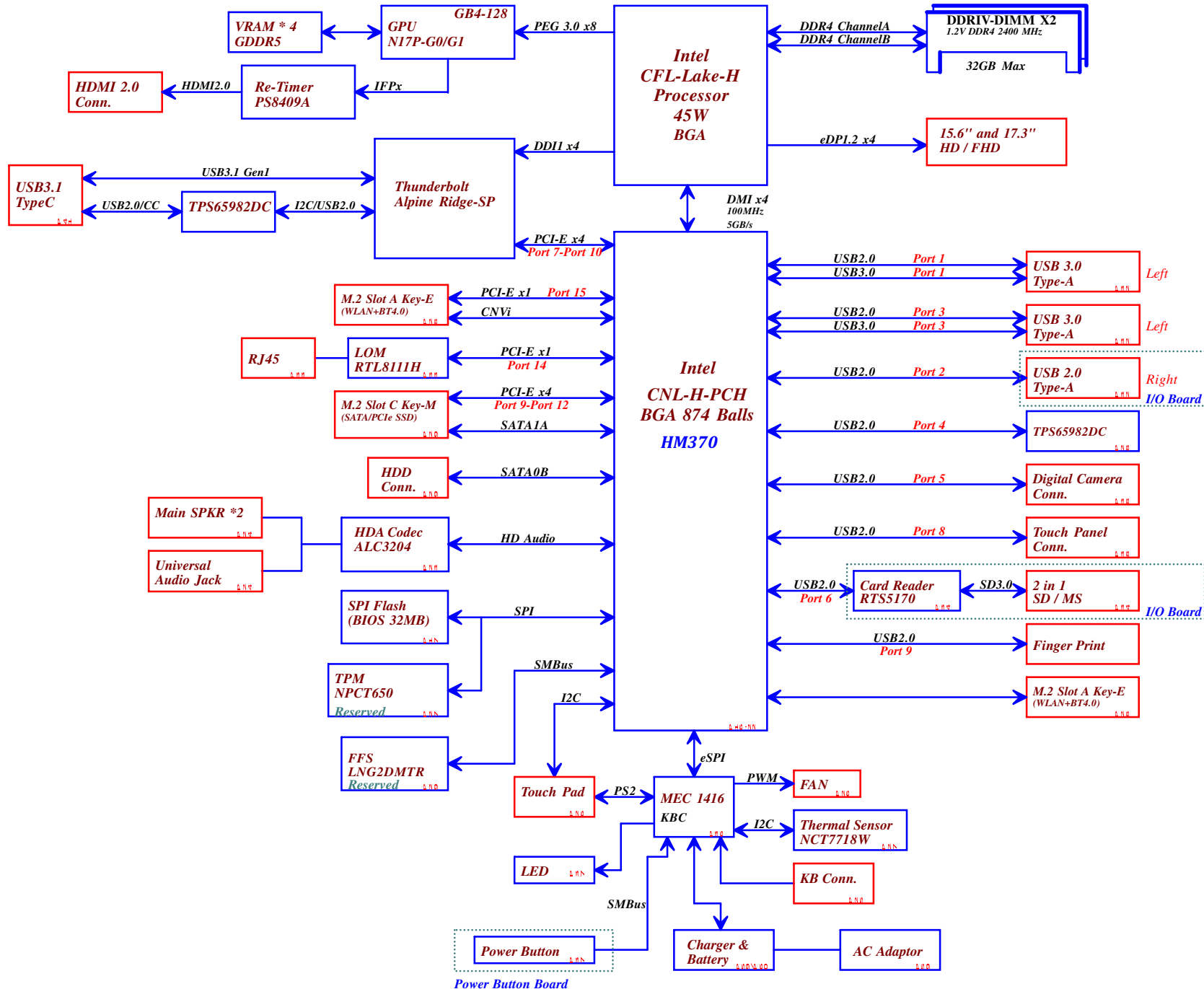
2018-03-22
REV : 1.0 (A00)

Layout Dell logo



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REV: X00
PWB: 9HTP8

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128M*32 x4 =2G
256M*32 x4 =4G

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Board ID	Resistor
X00	10K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

HSIO port Allocation

USB3	DESTINATION
1	USB JUSB1 (Left Side)
2	None
3	USB JUSB3 (Left Side)
4	None
5	None
6	None

USB2	DESTINATION
1	USB JUSB1 (Left Side)
2	USB JUSB2 (I/O)
3	USB JUSB3 (Left Side)
4	TYPE-C PD
5	CAMERA
6	Card Reader (I/O)
7	BT & CNVI BRI
8	Touch Screen
9	Finger Print
10	None
11	None
12	None
13	None
14	None

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	None	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9			
Lane 10			
Lane 11			
Lane 12			
Lane 13	None (HDD)		
Lane 14	LAN		
Lane 15	NGFF - WLAN		
Lane 16	None		
Lane 17	None		
Lane 18	None		
Lane 19	None		
Lane 20	None		
Lane 21			
Lane 22			
Lane 23			
Lane 24			

Table 1-7. PCH HSIO Detail (SKU 9-11 of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

13.2.1 Coffee Lake PCH-H

Figure 13-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	PCIe* #13	PCIe* #14
Intel® RST Support											No Support	No Support	Yes	No Support	Yes	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Symbol Note :

↓ : means Digital Ground

⏏ : means Analog Ground

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI2.0 LSPCON PS175

CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	TBT-AR	0	TBT-AR
1	None	1	None
2	None	2	None
3	None	3	None
4	None	4	None
5	None	5	None
6	None	6	None
7	GPU	7	GPU
8	None	8	None
9	NGFF - SSD	9	NVMe
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	LAN	14	LAN
15	WLAN	15	WLAN

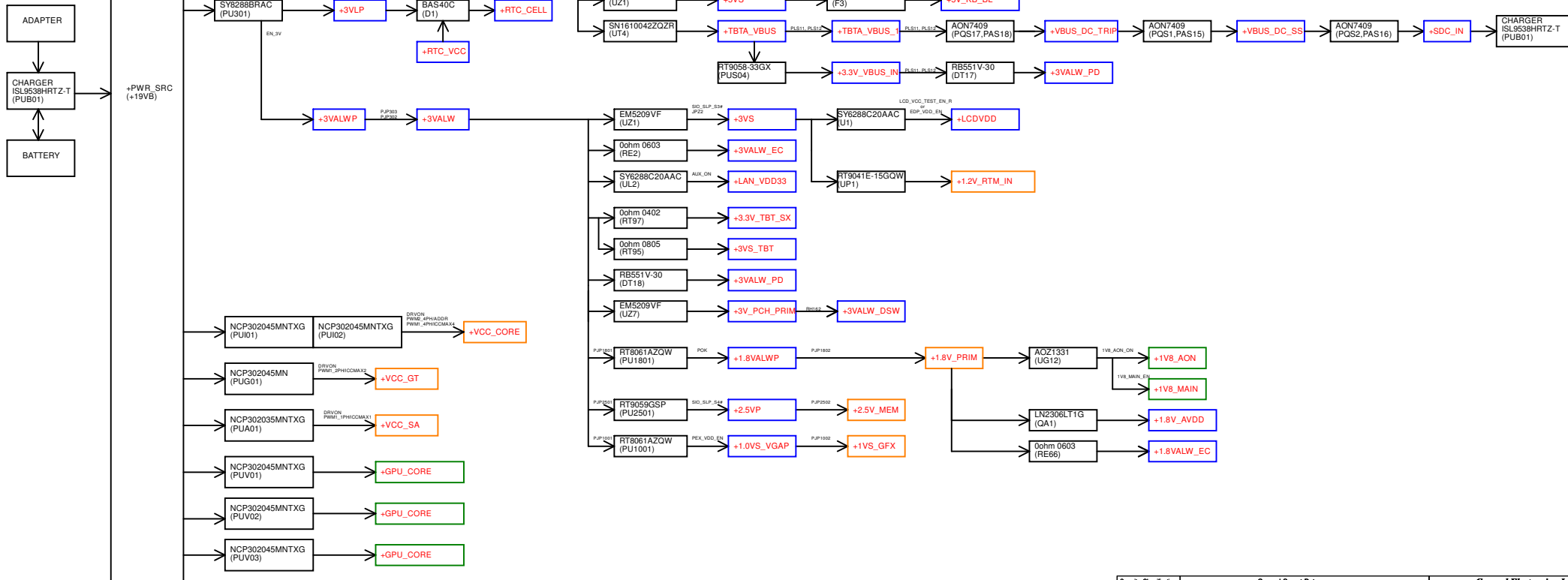
eSPI Virtual Wires (VW) (Sheet 1 of 2)

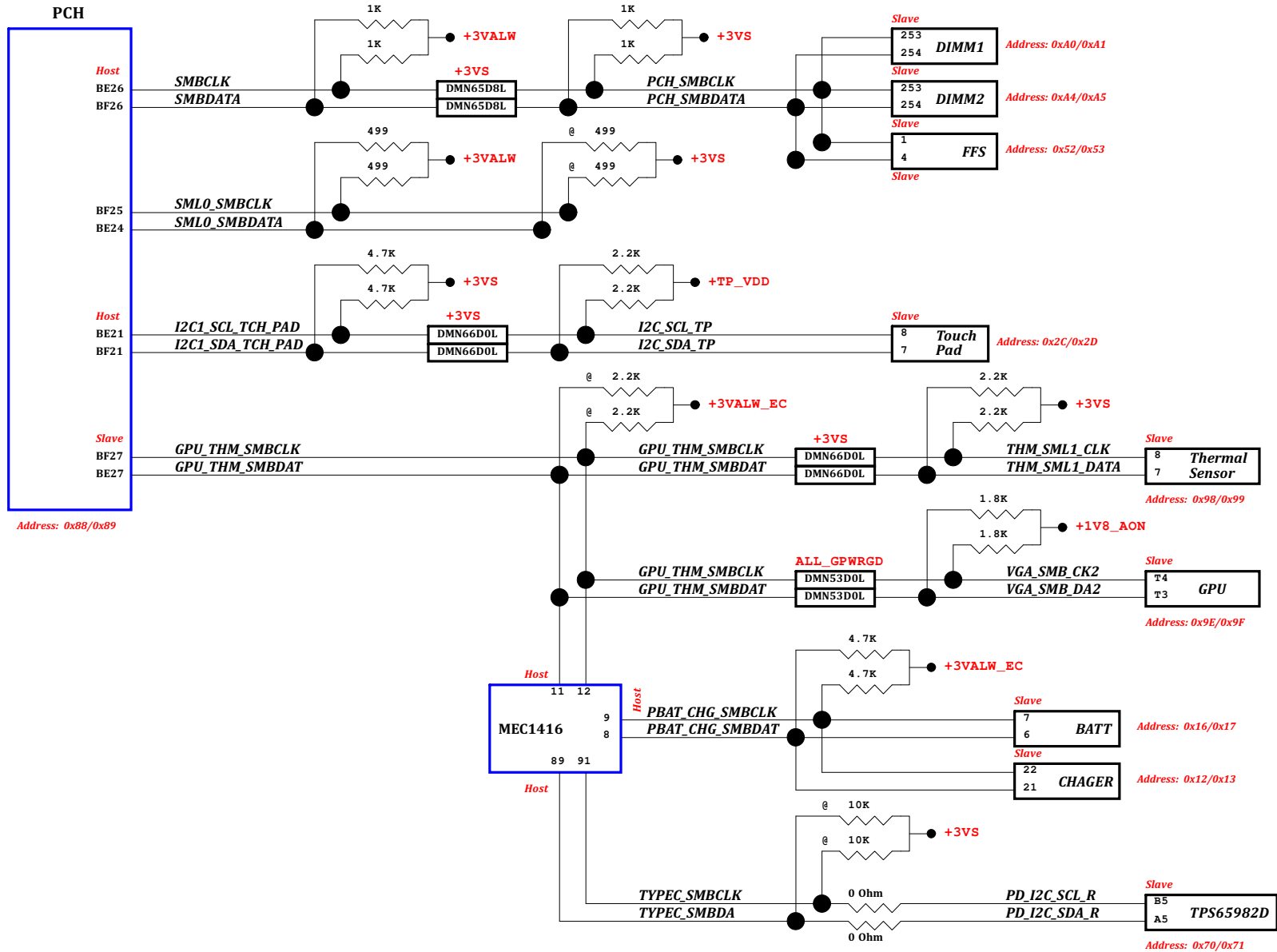
Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

eSPI Virtual Wires (VW) (Sheet 2 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_S5#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes

CPU PWR
GPU PWR
Peripheral Device PWR





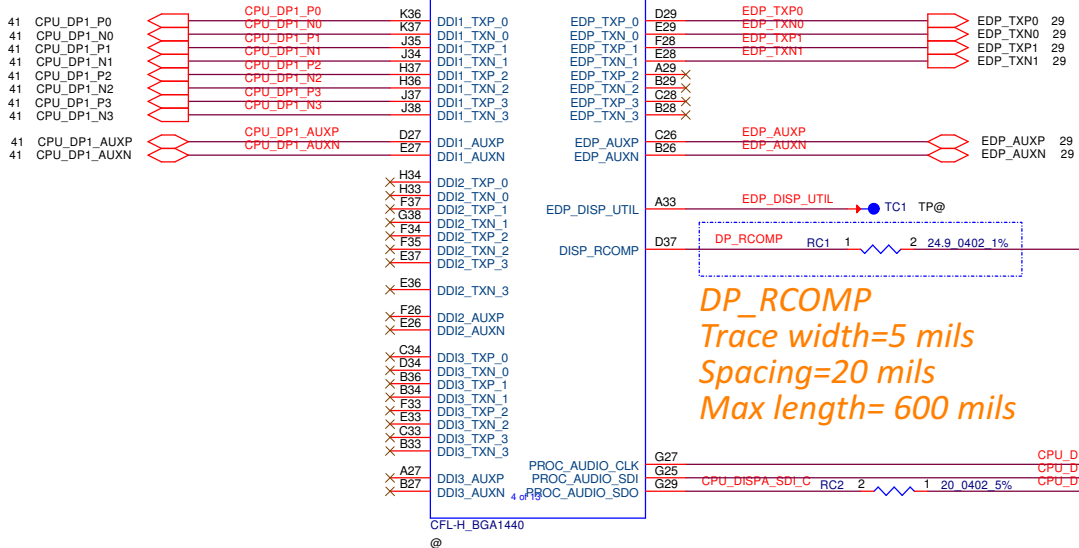
Main Func = CPU

TBT-AR



CFL_H_SOC

UC1D



eDP

+VCCIO

Check OK

DP_RCOMP

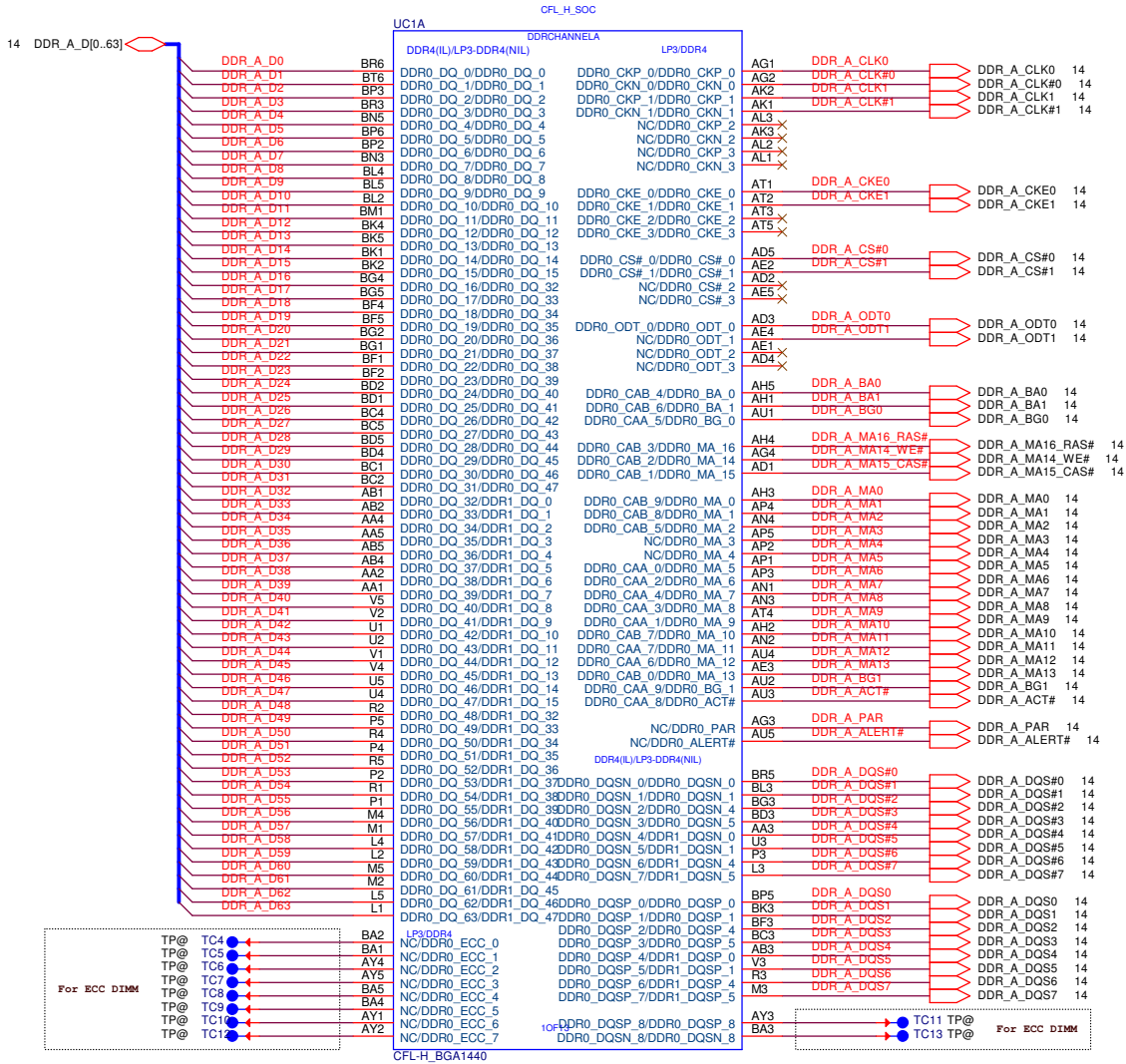
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Spacing=20 mils

Max length= 600 mils

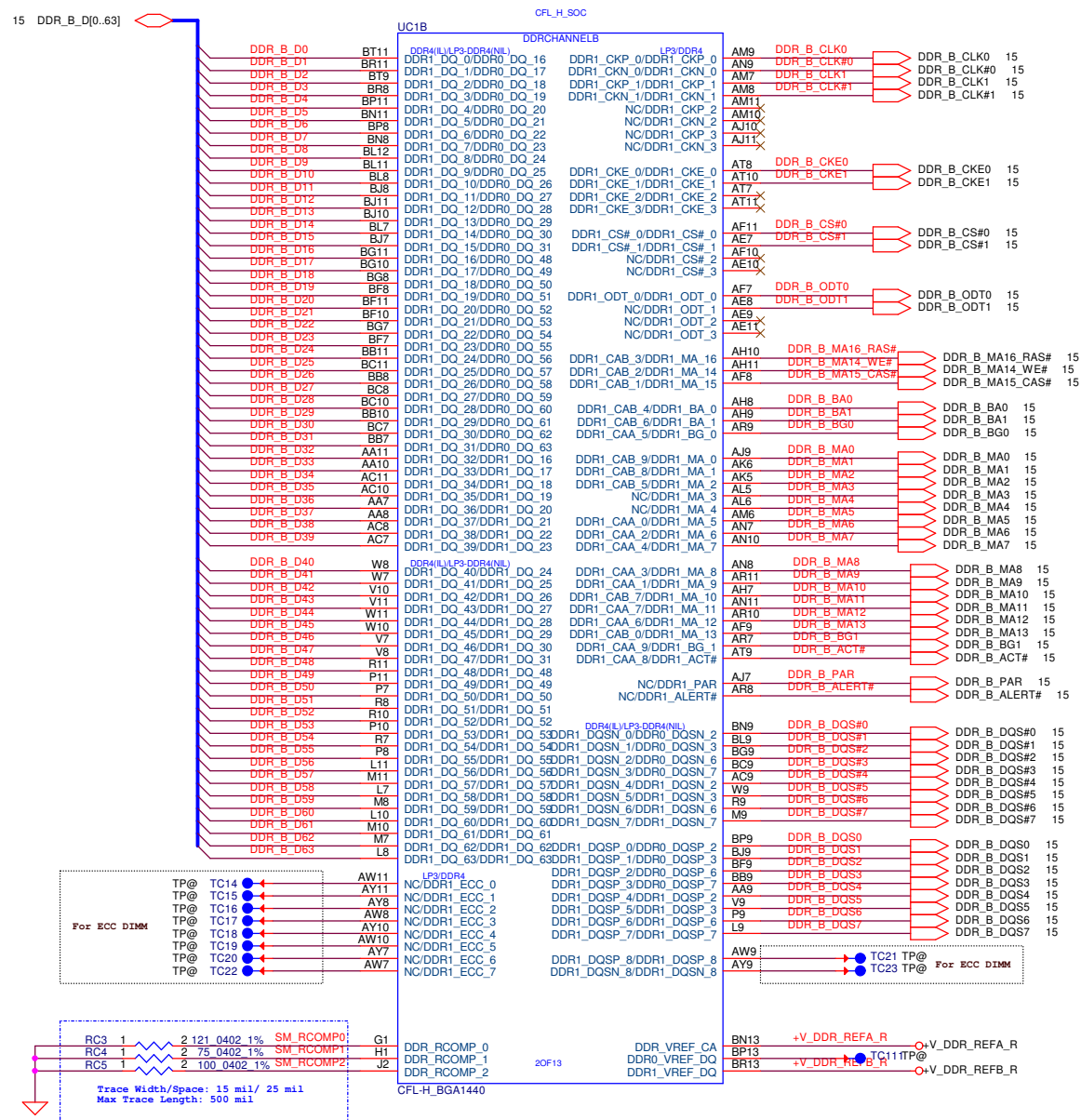
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								Size		Document Number		Rev	
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								Date:		Thursday, March 22, 2018		Sheet 6 of 78	

Main Func = CPU



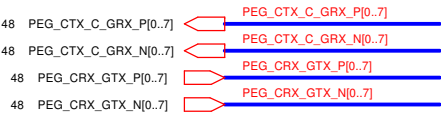
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Main Func = CPU



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Main Func = CPU



+VCCIO

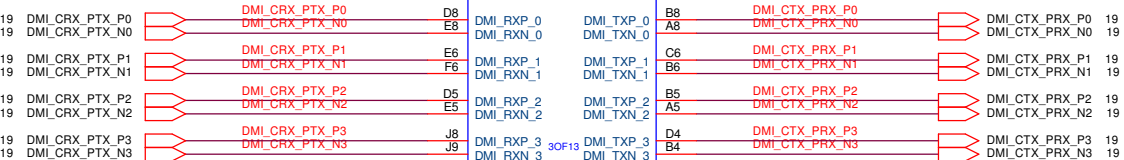
RC9 1 2 24.9 0402 1%

PEG_RCOMP

Trace Width/Space: 15 mil/ 15 mil

Max Trace Length: 600 mil

G2 PEG_RCOMP



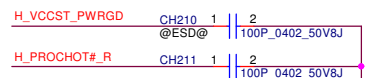
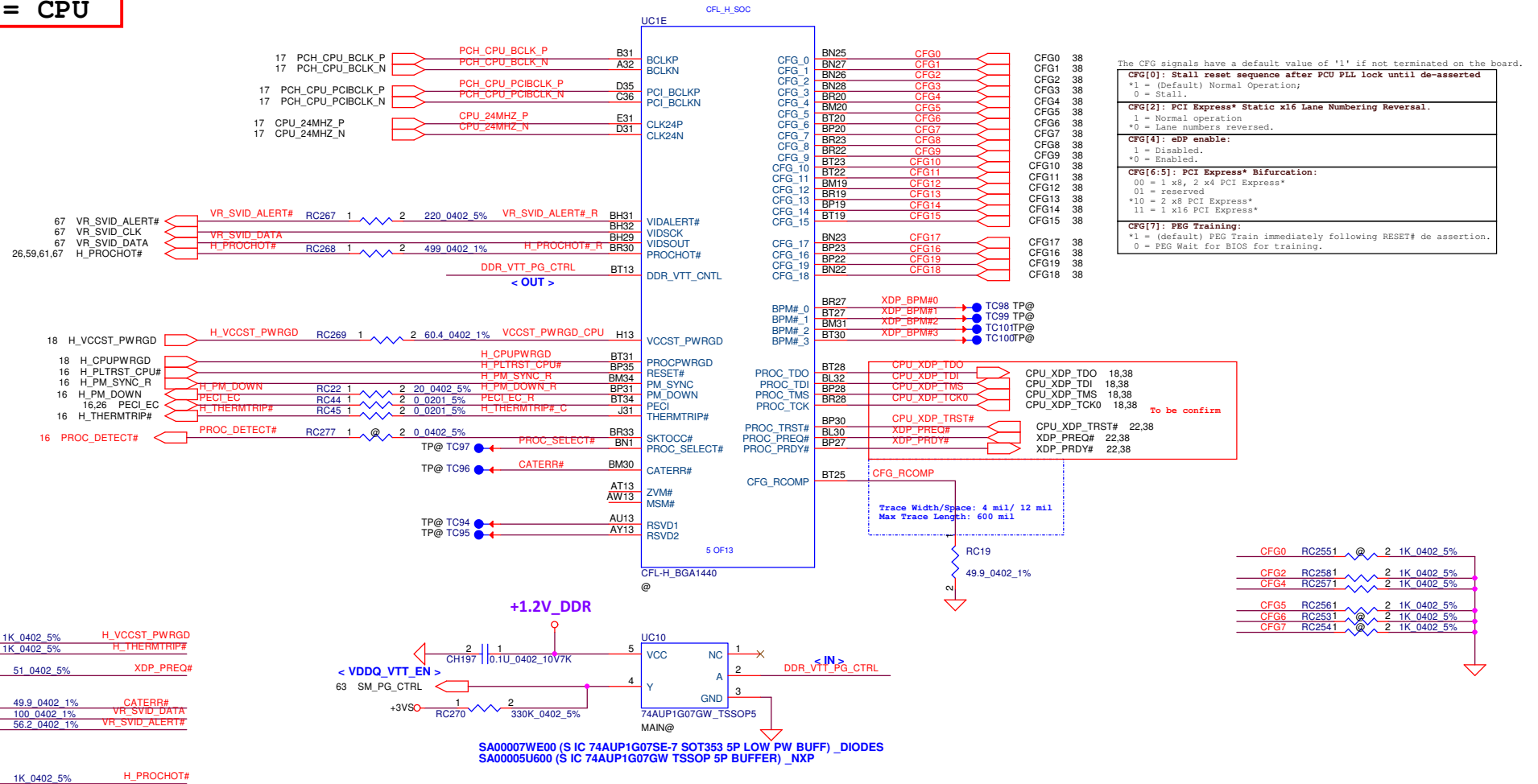
PEG_RCOMP

Trace width=15 mils

Spacing=15 mils

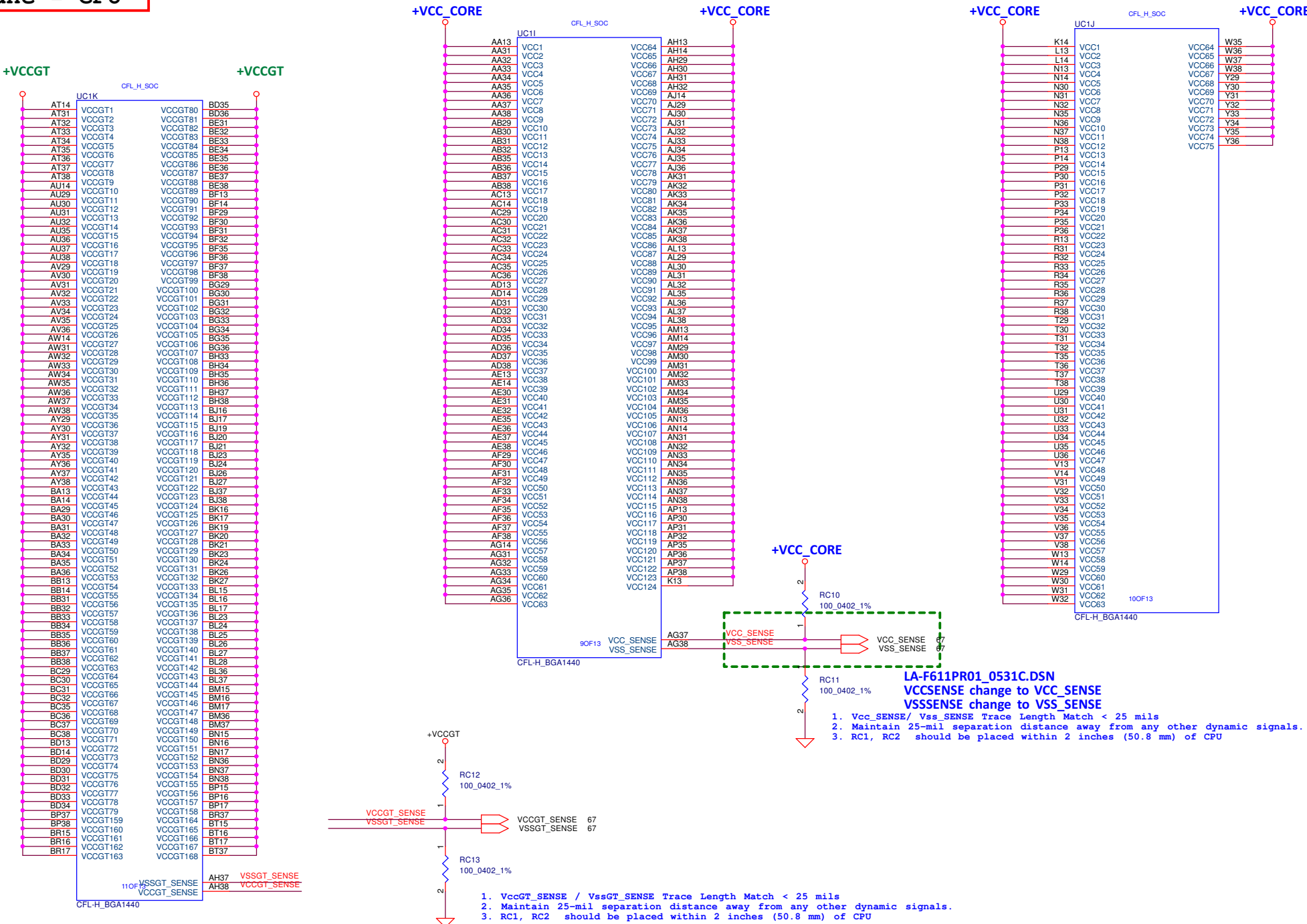
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Main Func = CPU



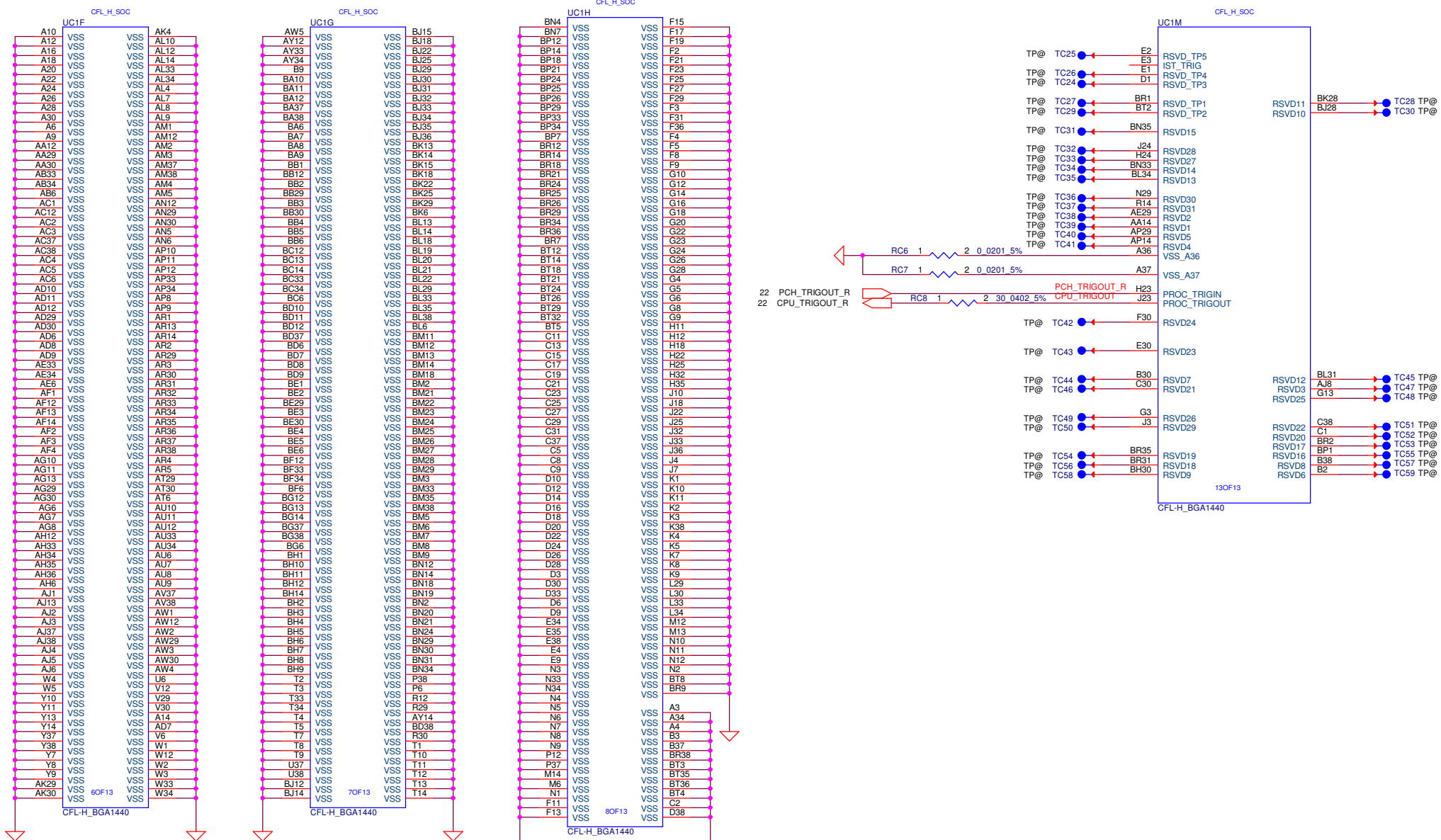
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Main Func = CPU



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								LA-F611P		0.3			
								Date:		Thursday, March 22, 2018		Sheet 11 of 78	

Main Func = CPU

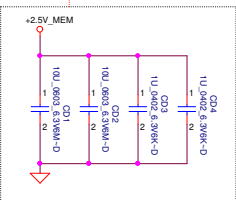


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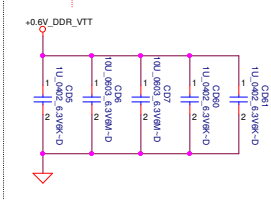
Main Func = DDR

7 DDR_A_D0[0..63]
7 DDR_A_M0[0..13]
7 DDR_A_DQS[0..7]
7 DDR_A_DQS[0..7]

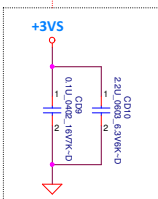
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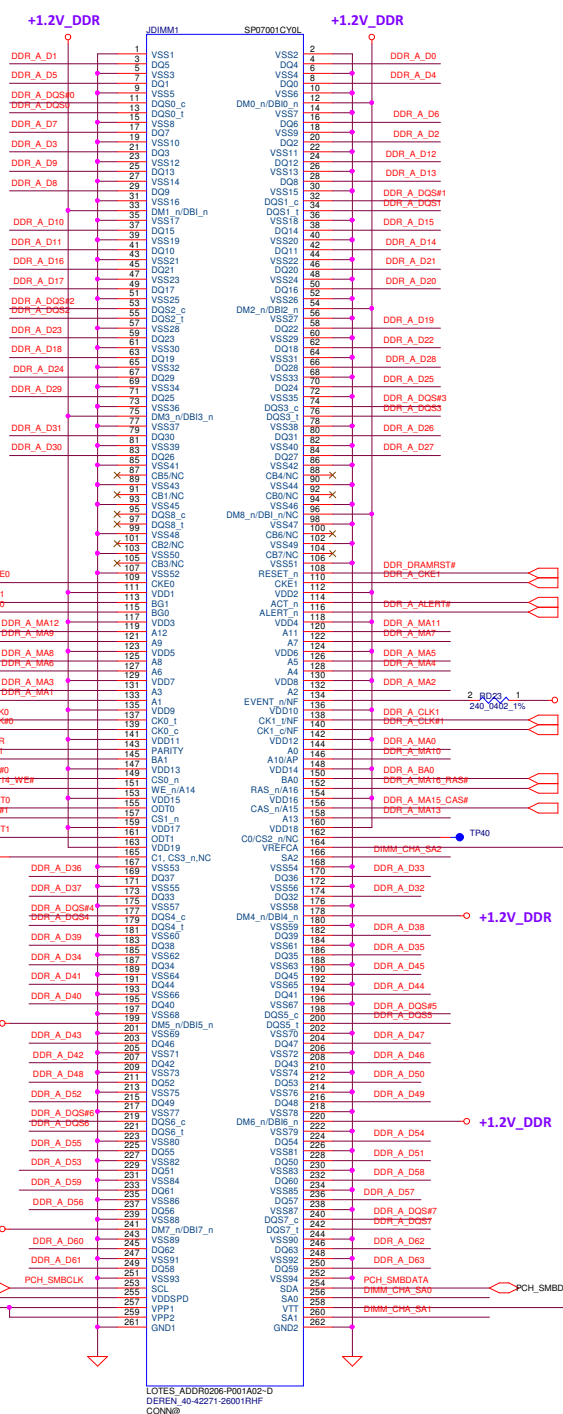
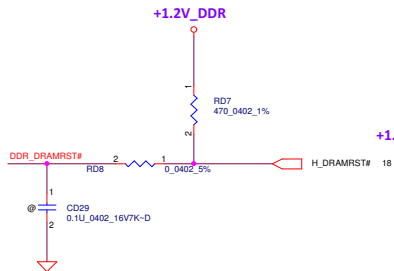
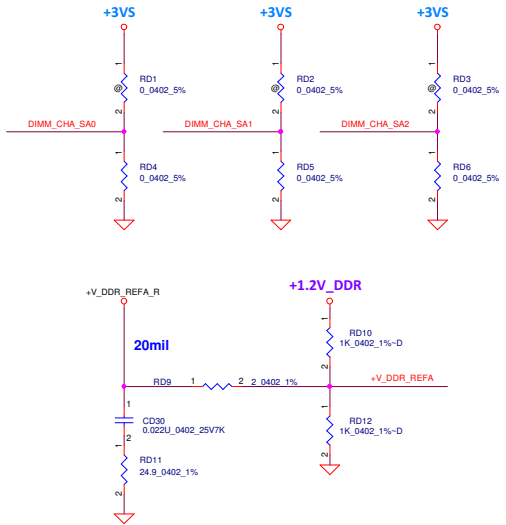
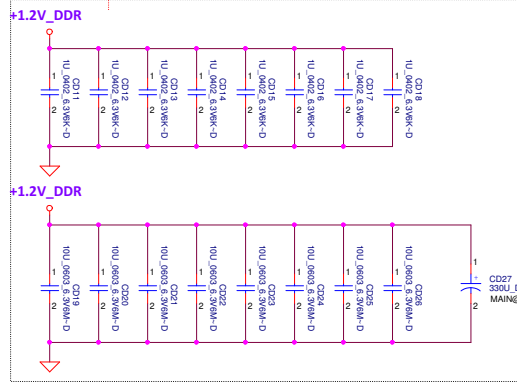
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Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1



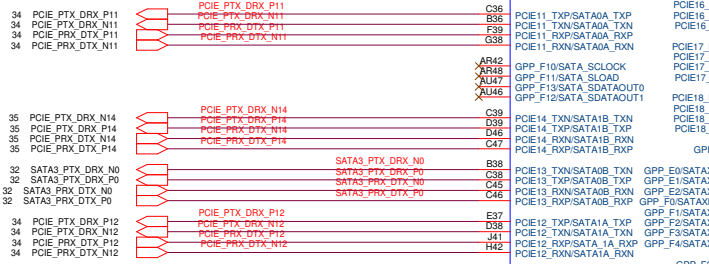
All VREF traces should
have 10 mil trace width



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ¹	None ²	None ³

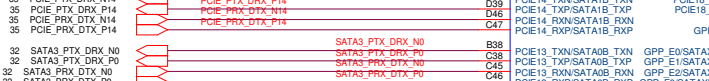
PCIe SSD
M.2 SSD/ NVMe/ Optane
PCIe



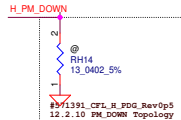
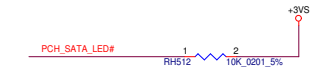
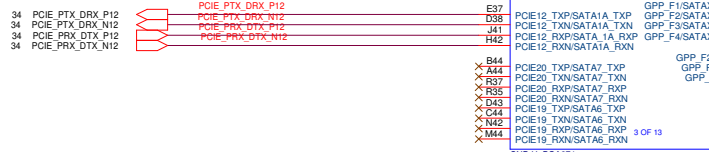
PCIe SSD
M.2 SSD/ NVMe/ Optane
PCIe / SATA

WLAN

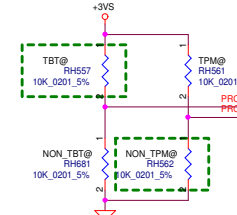
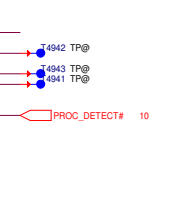
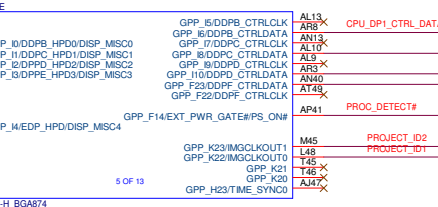
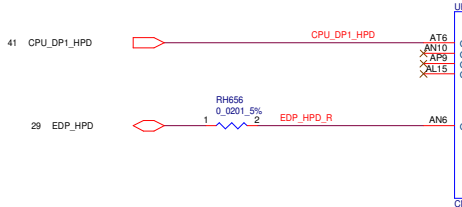
LAN



PCIe SSD
M.2 SSD/ NVMe/ Optane
PCIe



eDP_HP_D pull down 100K



PROJECT ID	PROJECT ID1 (GPP_K22)
Non-TBT	0
TBT	1

TPM ID	PROJECT ID2 (GPP_K23)
SW TPM	0
HW TPM	1

PCH Strap PIN



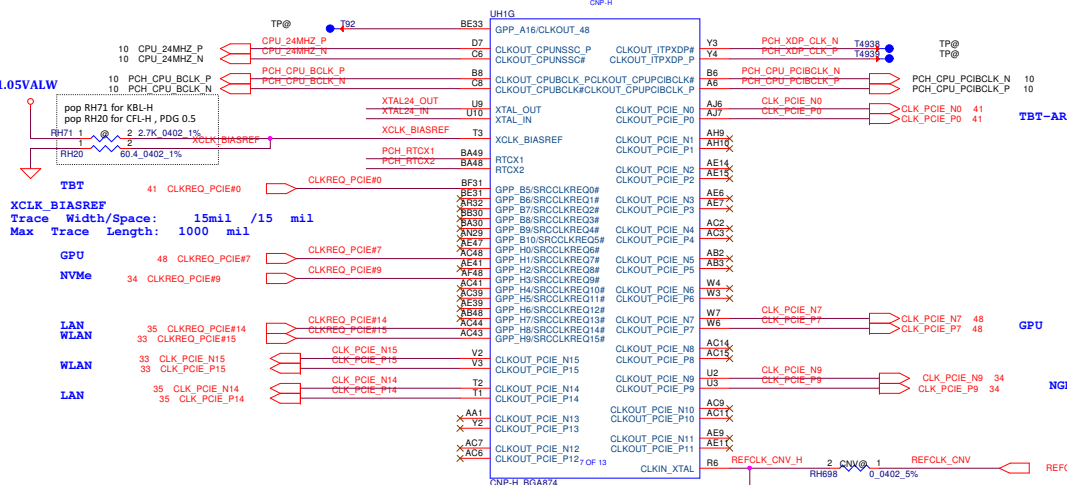
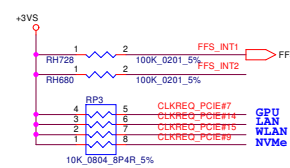
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.
Notes:
1. This internal Pull-down is disabled after PCH_PWROR de-asserts.
2. This signal is in the primary wall.

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Lane #1										USB3.1 Gen1/Lane #2										USB3.1 Gen1/Lane #3										USB3.1 Gen1/Lane #4										USB3.1 Gen1/Lane #5										USB3.1 Gen1/Lane #6										USB3.1 Gen1/Lane #7										USB3.1 Gen1/Lane #8										USB3.1 Gen1/Lane #9										USB3.1 Gen1/Lane #10										PCIe #1										PCIe #2										PCIe #3										PCIe #4										PCIe #5										PCIe #6										PCIe #7										PCIe #8										PCIe #9										PCIe #10										PCIe #11										PCIe #12										PCIe #13										PCIe #14										PCIe #15										PCIe #16										PCIe #17										PCIe #18										PCIe #19										PCIe #20										PCIe #21										PCIe #22										PCIe #23										PCIe #24										PCIe #25										PCIe #26										PCIe #27										PCIe #28										PCIe #29																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									
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DisplayPort* Disabling and Termination Guidelines

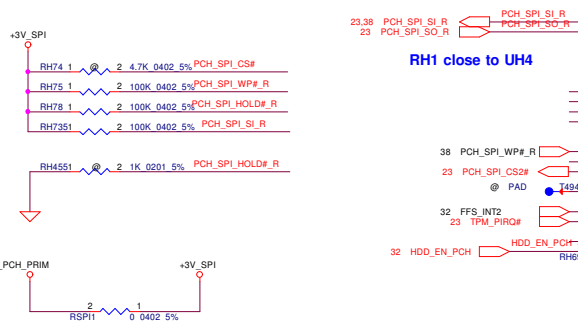
Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

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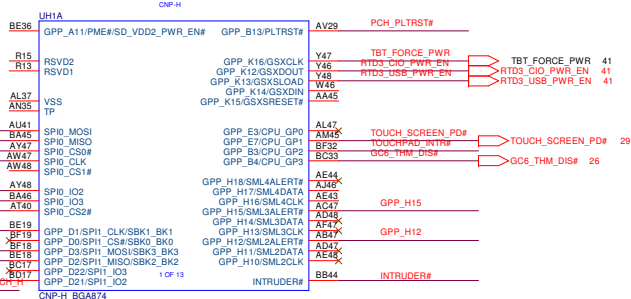


CFL-H PDG rev0.7
pop 20K for SPI0_IO2/3

CNL- PCH EDS rev0.5
Reserved External pull-up is required. Recommend 100K if pulled
up to 3.3V

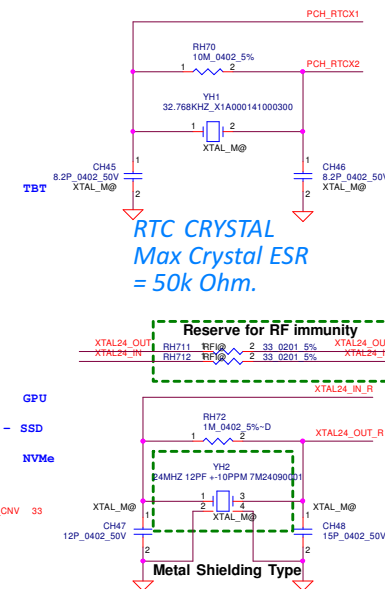


RH1 close to UH4



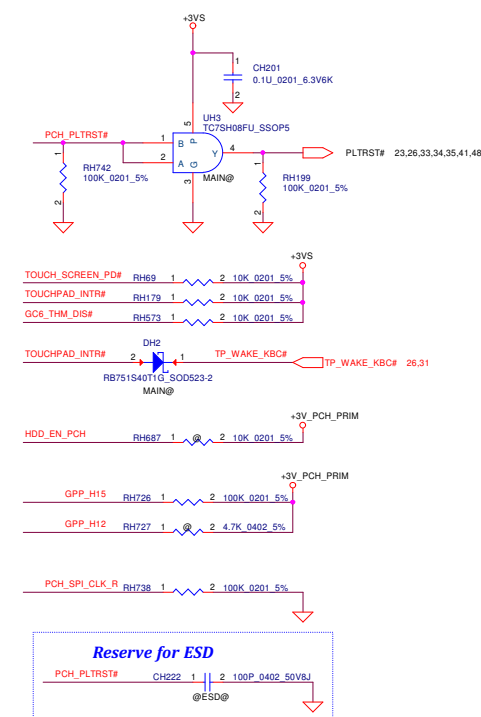
SPI ROM

PCH

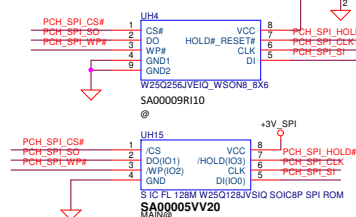


YH1 CH45 CH46 Main X76 control
X7676731L91

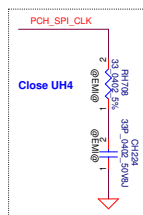
YH2 CH47 CH48 Main X76 control
X7676731L74



Reserve for ESD

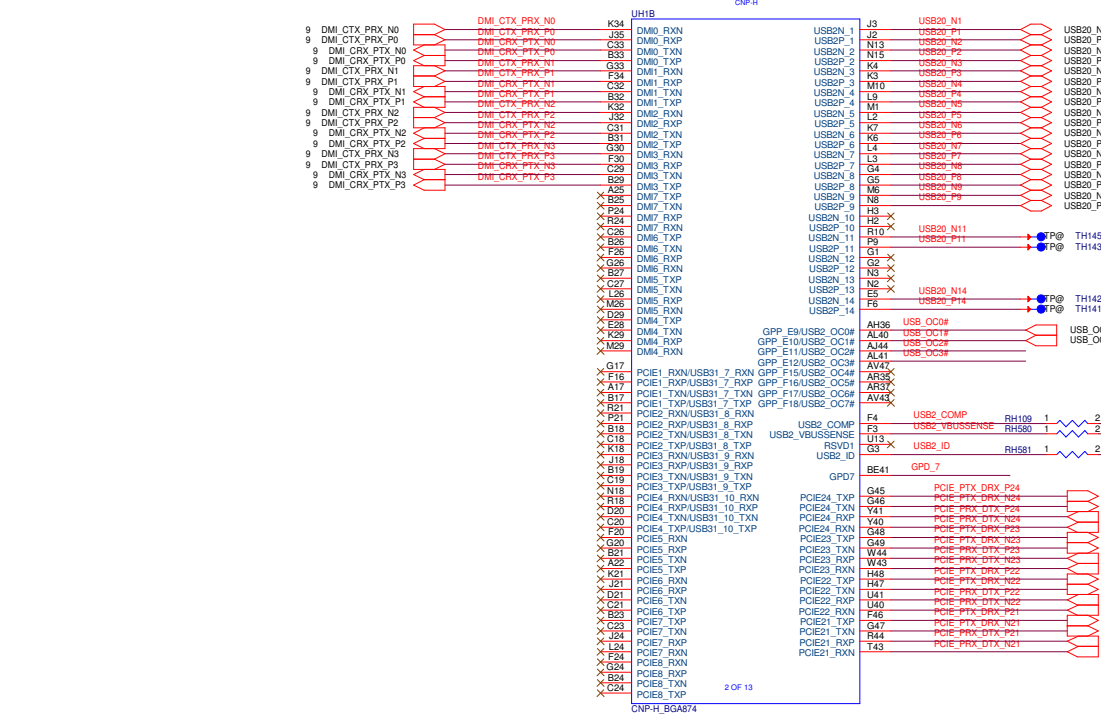


Co-lay with UH4

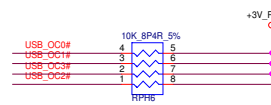


Security Classification	Compel Secret Data		Compel Electronics, Inc. PCH (2/7) CLK,SPI,PLTRST	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title LA-F611P Date: July 22, 2018
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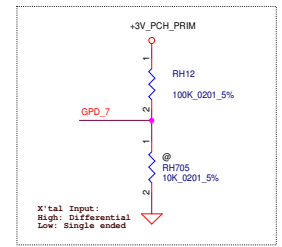


- > Port 1, USB3.0 (MB)
- > Port 3, USB2.0 (IO/B)
- > Port 2, USB3.0 (MB)
- > TYPEC PD
- > CCD
- > Card Reader (IO/B)
- > BT & CNVI BRI use
- > Touch Screen
- > Finger Printer

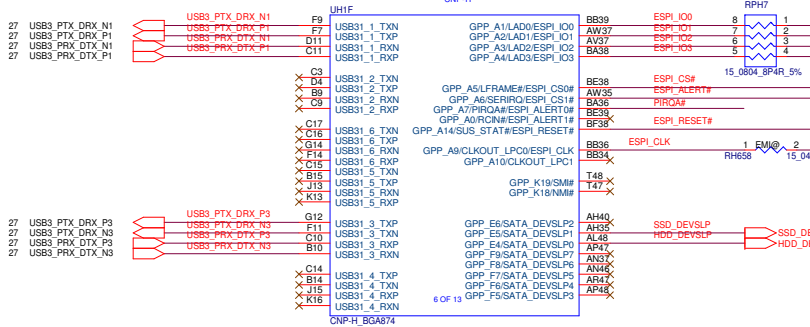


USB2_COMP
50ohm single-ended and as short as possible
Spacing=15 mils
Max length= 1000 mils

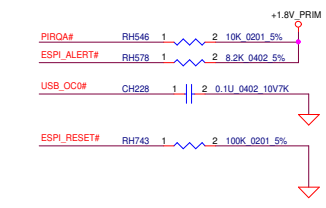
TBT-AR



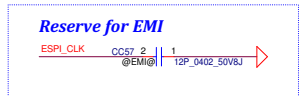
USB3.0 Port1



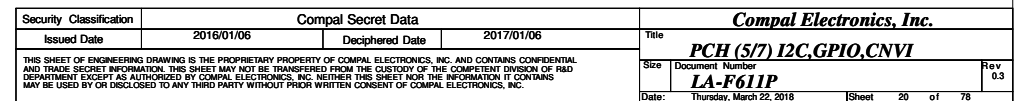
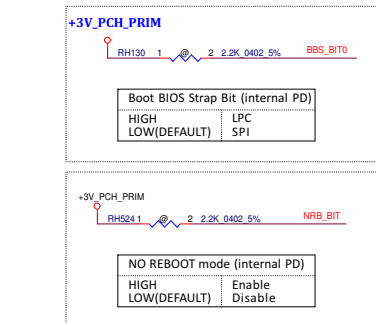
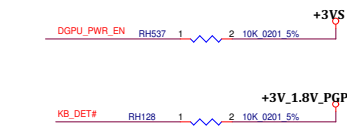
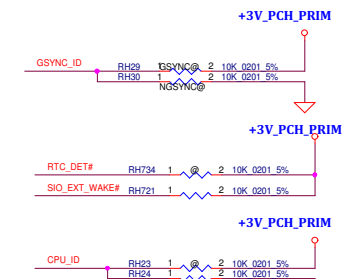
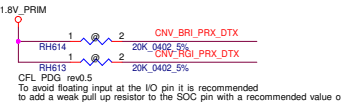
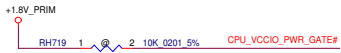
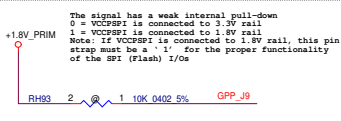
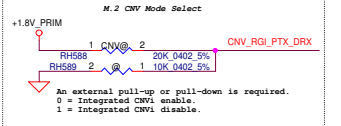
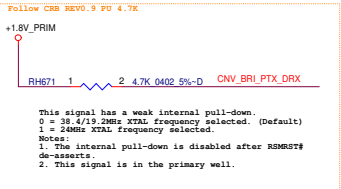
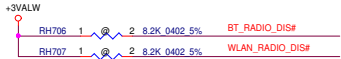
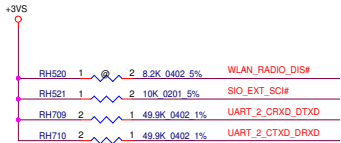
USB3.0 Port2



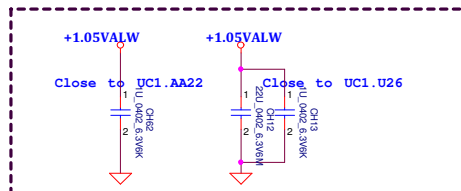
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #7	USB3.1 Gen1/Gen2 #8	USB3.1 Gen1/Gen2 #9	USB3.1 Gen1/Gen2 #10	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support



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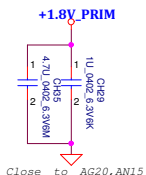
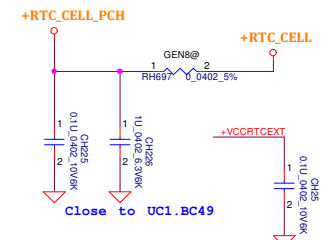
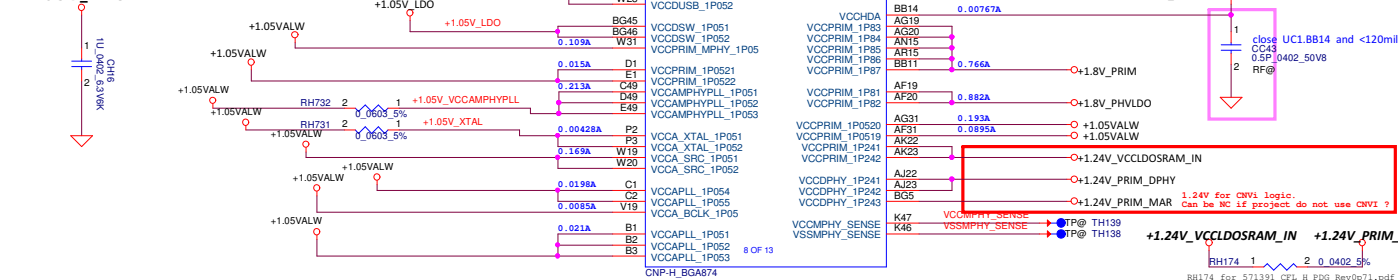


Main Func = PCH

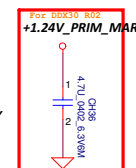


PLACE 3-5MM FROM PACKAGE EDGE

Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.



Close to AG20, AN15



For DDX30 R02
+1.24V PRIM MAR

+1.24V VCCLDOSRAM IN +1.24V PRIM DPHY

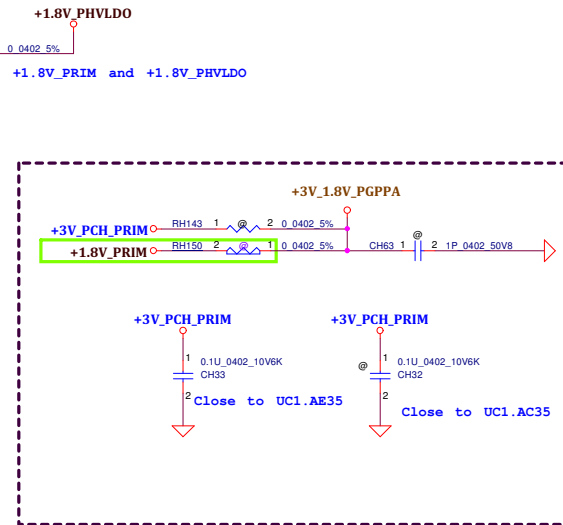
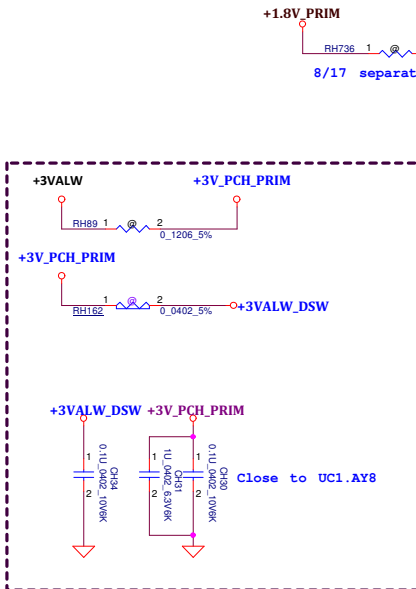
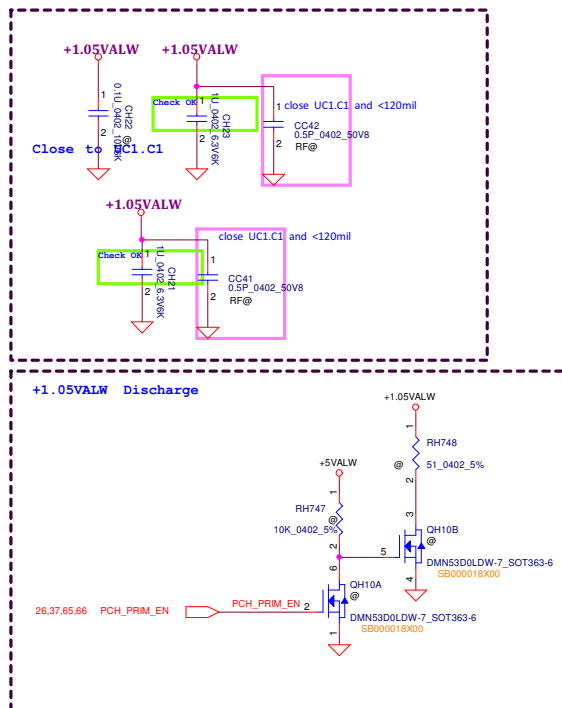
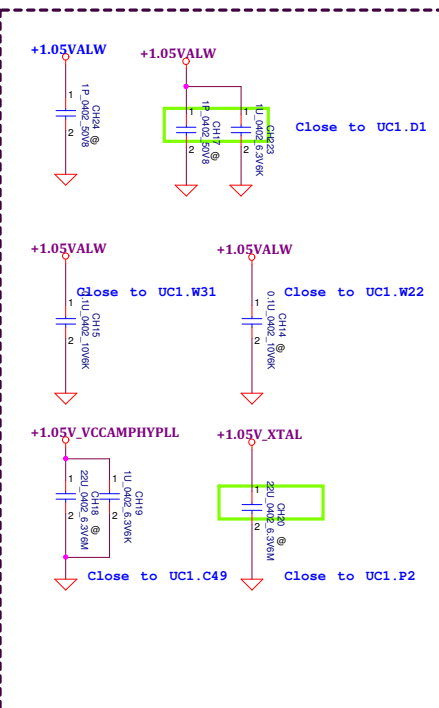
1.24V for CNVi logic.
Can be 1.2V if product do not use CNVi.

Can be NO if project do not use CNVI

24V VCCLDOSRAM IN +1.24V PRIM

PU174 1 2 0.0400 5N

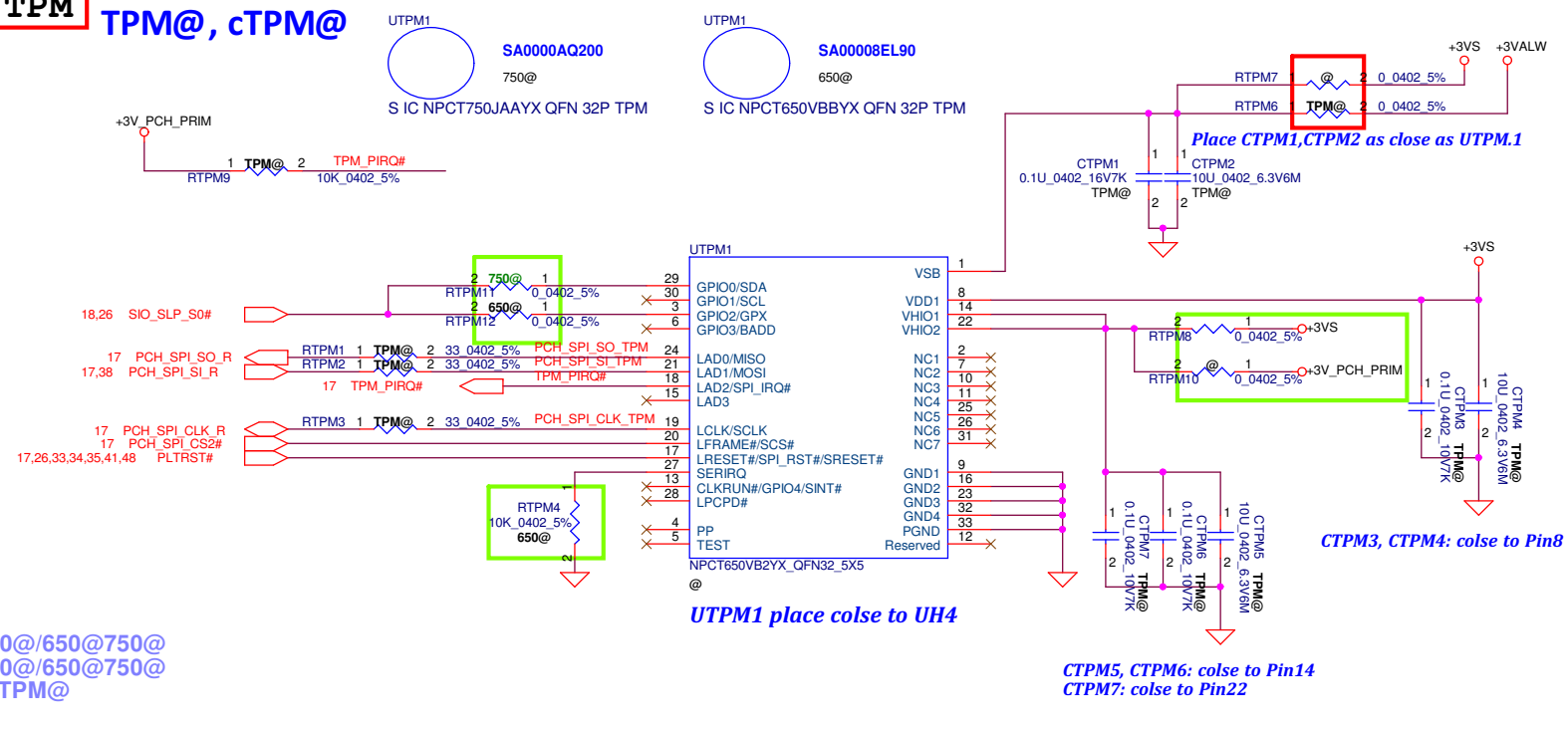
BH174 for 571391 CFL H PDG Rev0p71.pc



Security Classification		Compal Secret Data		Compal Electronics, Inc. PCH (6/7) POWER	
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				LA-F611P	
				Date:	Thursday, March 22, 2018
				Sheet	21 of 78

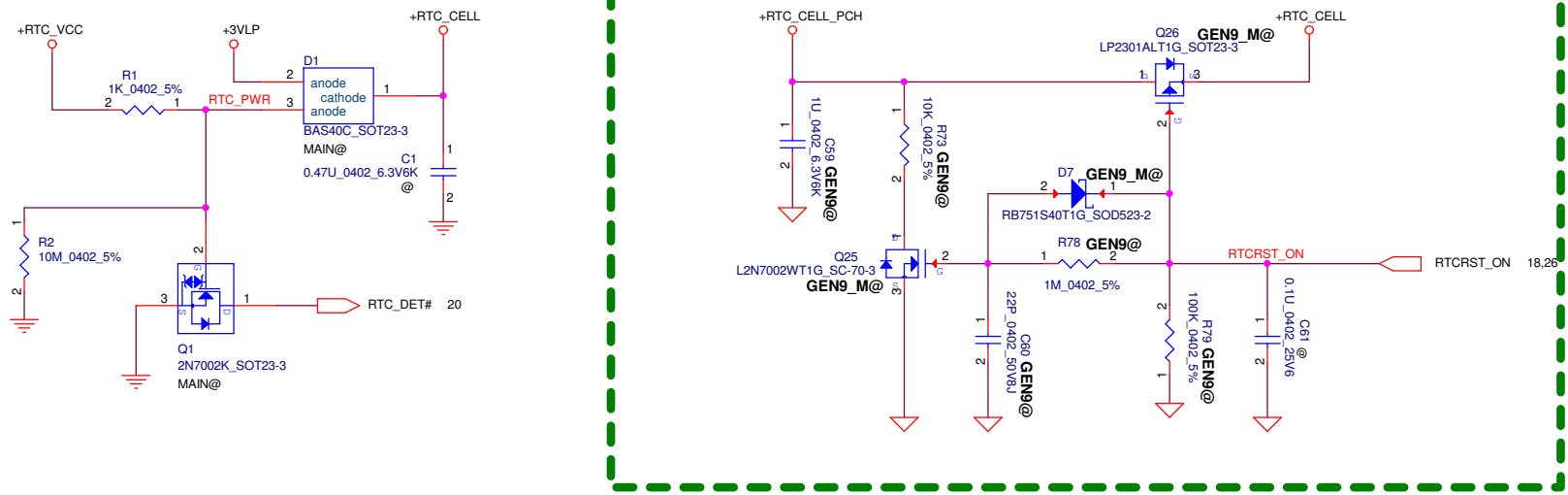
Main Func = TPM

TPM@, cTPM@

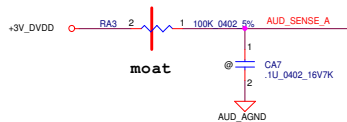
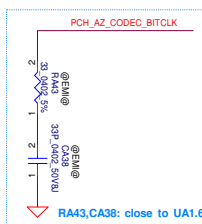
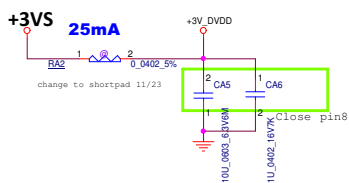
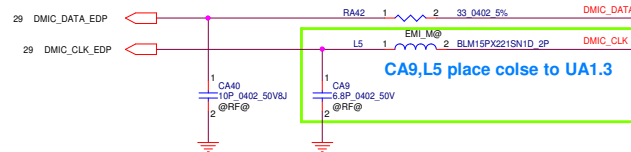
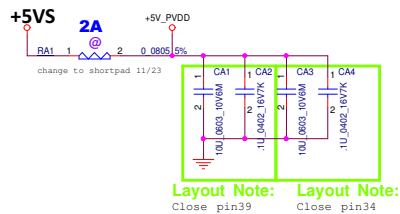


Main Func = RTC

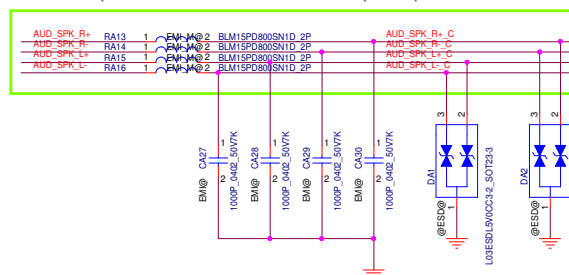
GEN9@



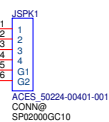
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Issued Date		2016/01/06		Deciphered Date		2017/01/06		Title					
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								Size		Document Number		Rev	
								LA-F611P		0.3			
								Date:		Thursday, March 22, 2018		Sheet	
								23		of		78	



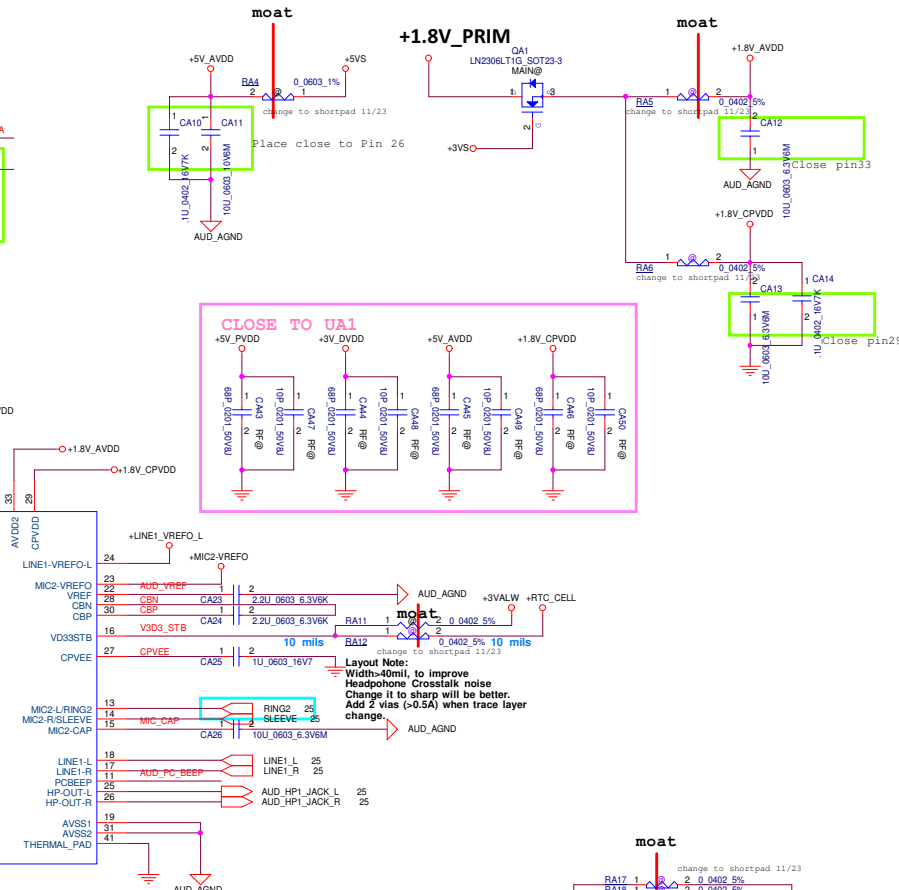
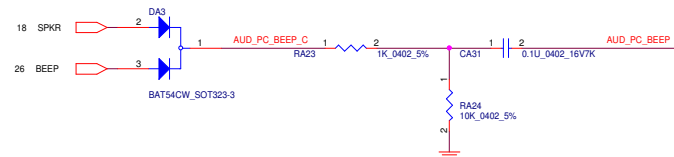
Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power



Speaker



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



ESD@

Layout Note:
Close to UA1

EMI@, @ESD@, ESD@

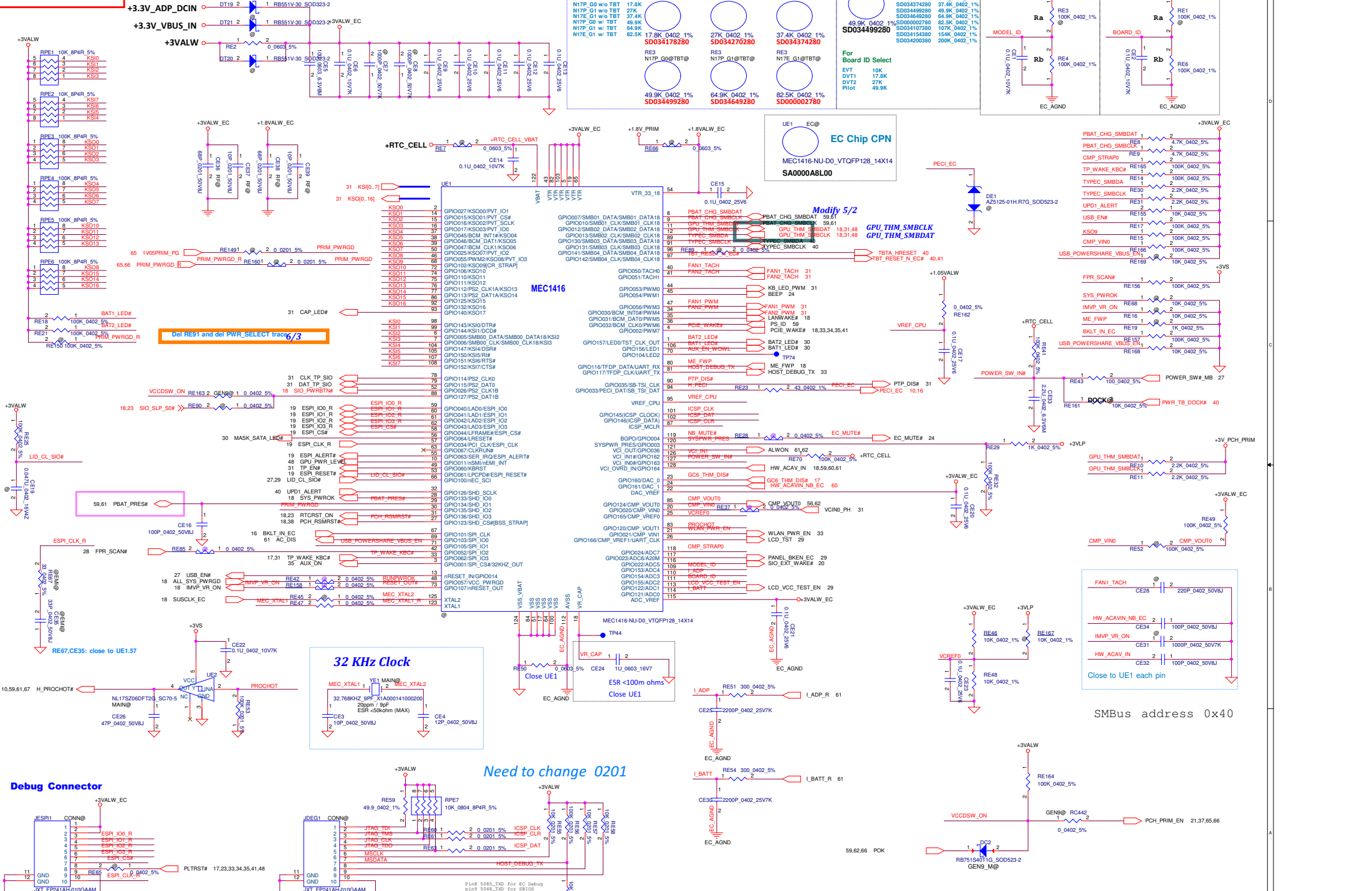
Security Classification

Compal Secret Data

Compal Electronics, Inc.

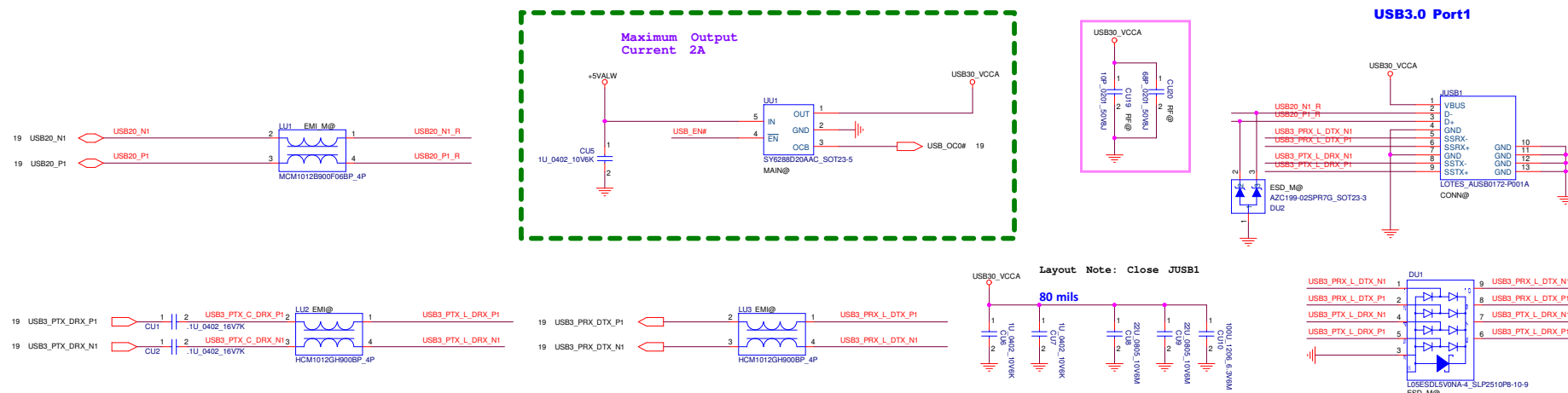
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title		
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				Size	Document Number	Rev. 0.3
				LA-F611P		
				Date:	Thursday, March 22, 2018	Sheet 25 of 78

Main Func = EC

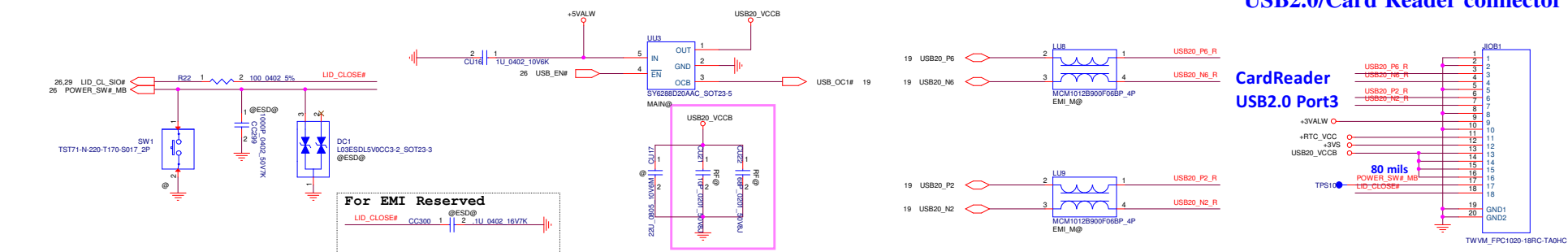


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				Date:	Thursday, March 22, 2018	
				Sheet	26 of 78	

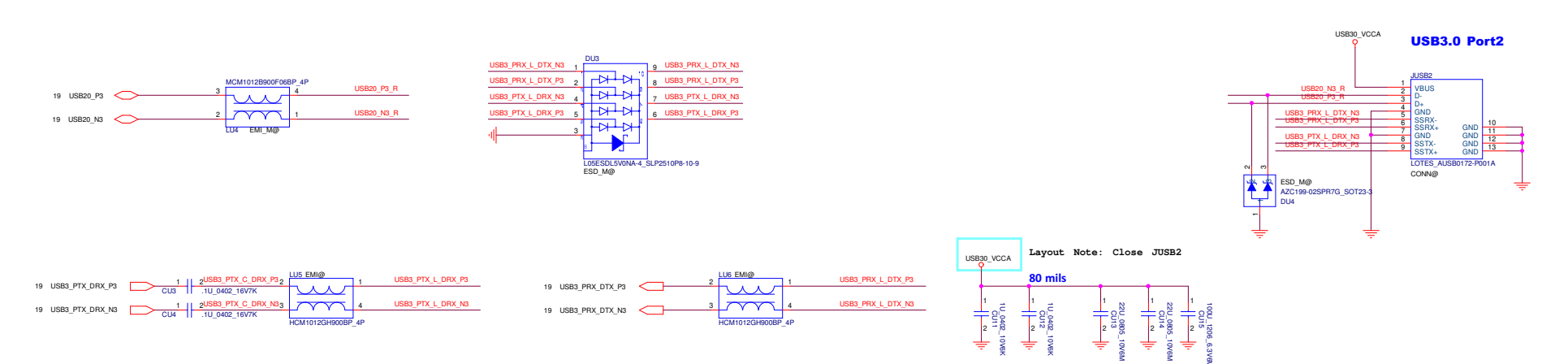
Main Func = USB3.0 Port1



Main Func = USB2.0 Port2 + Card Reader+Power BTN on IO/B

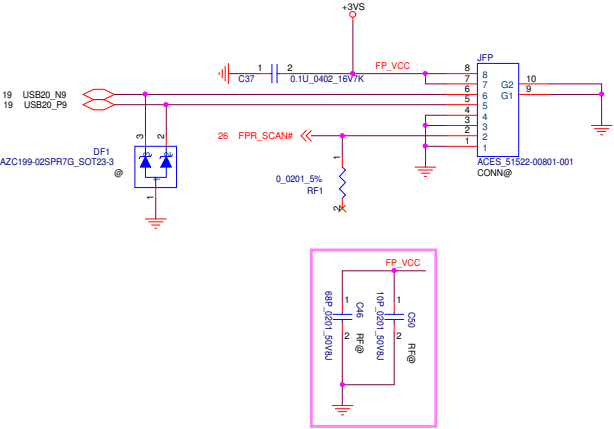


Main Func = USB3.0 Port2



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				Sheet	27 of 78

Main Func = Finger Printer

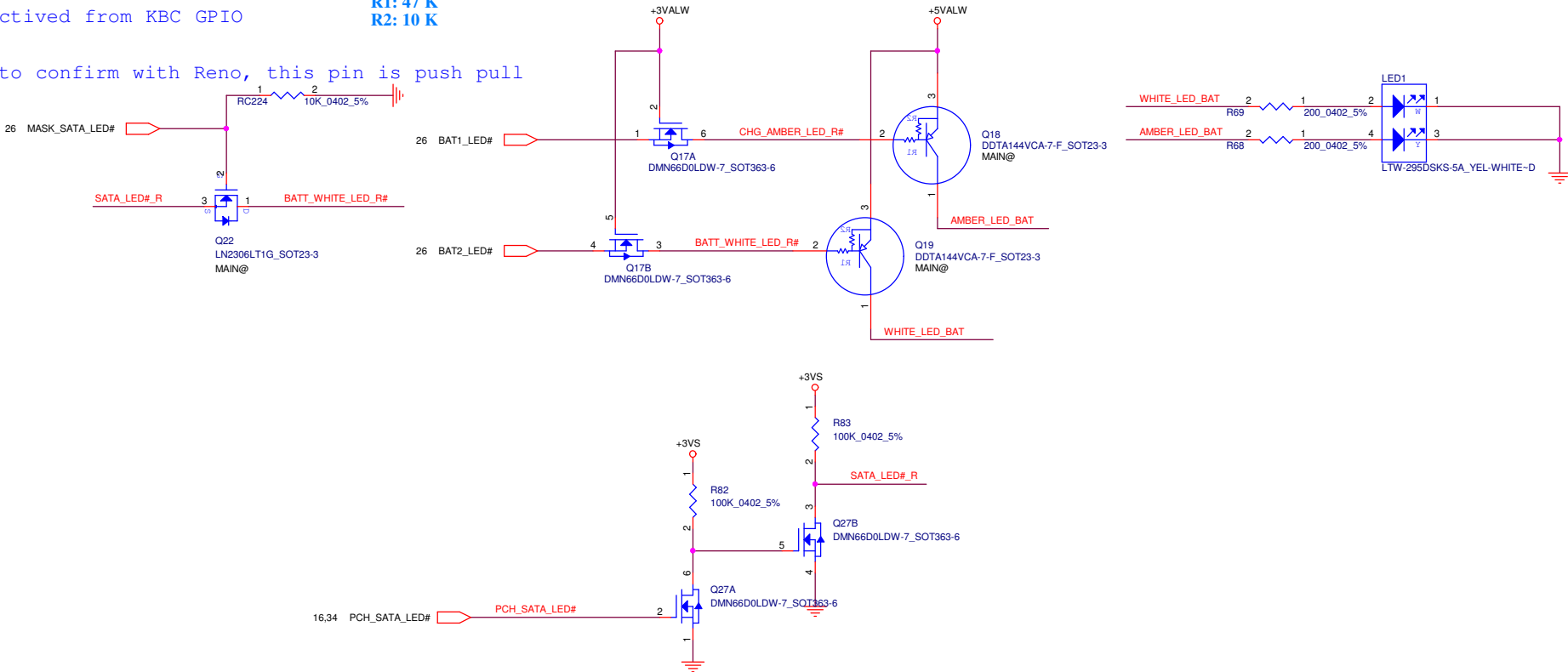


Main Func = Battery LED

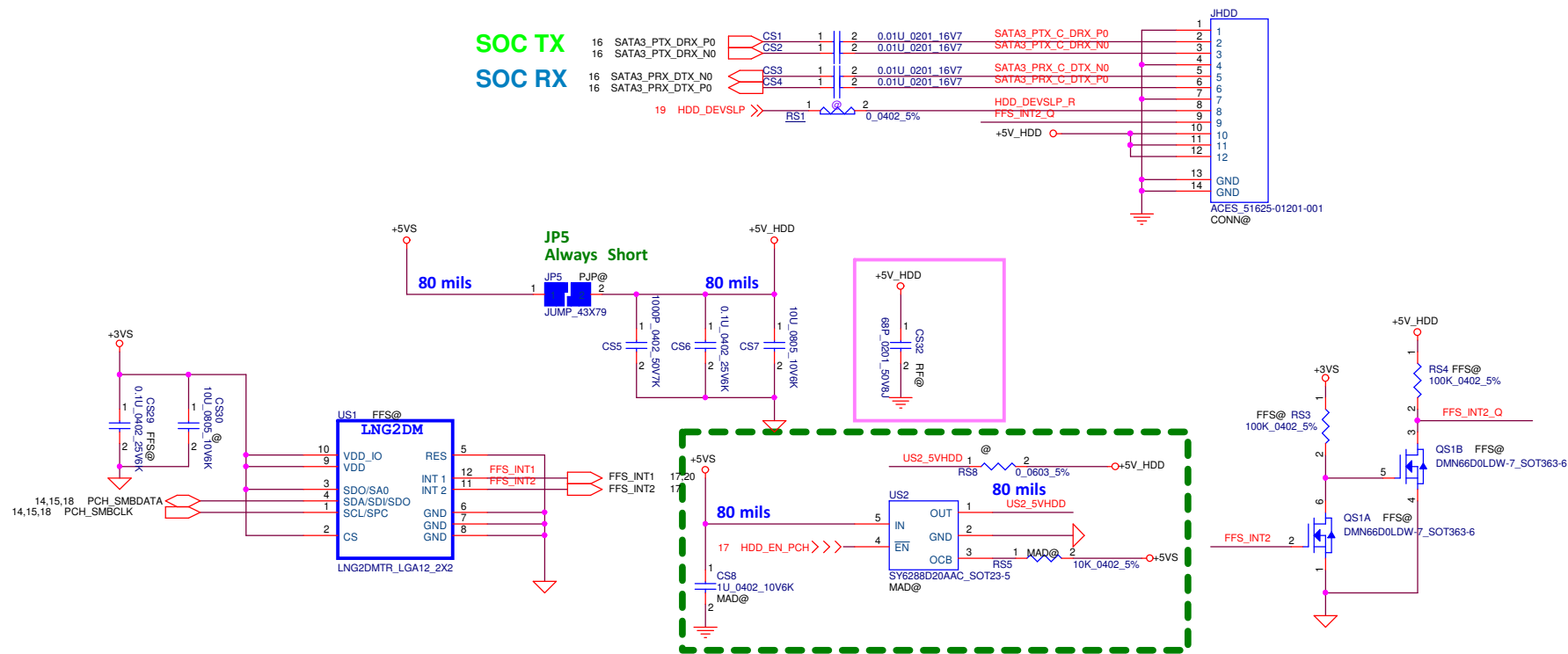
Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K

Need to confirm with Reno, this pin is push pull



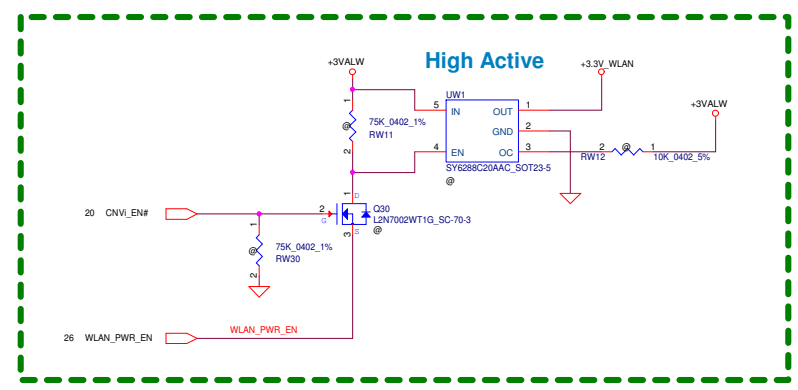
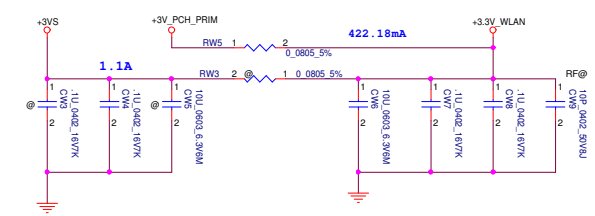
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title Power Button/LED	
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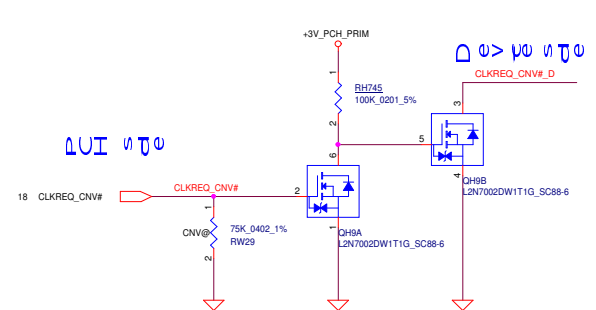
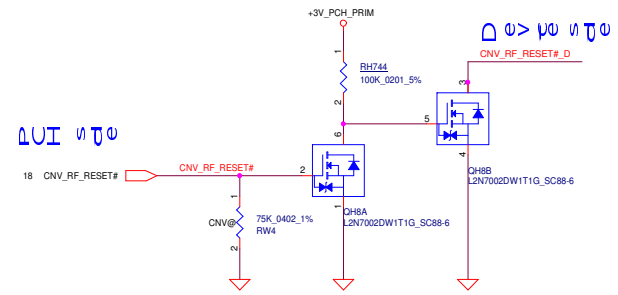
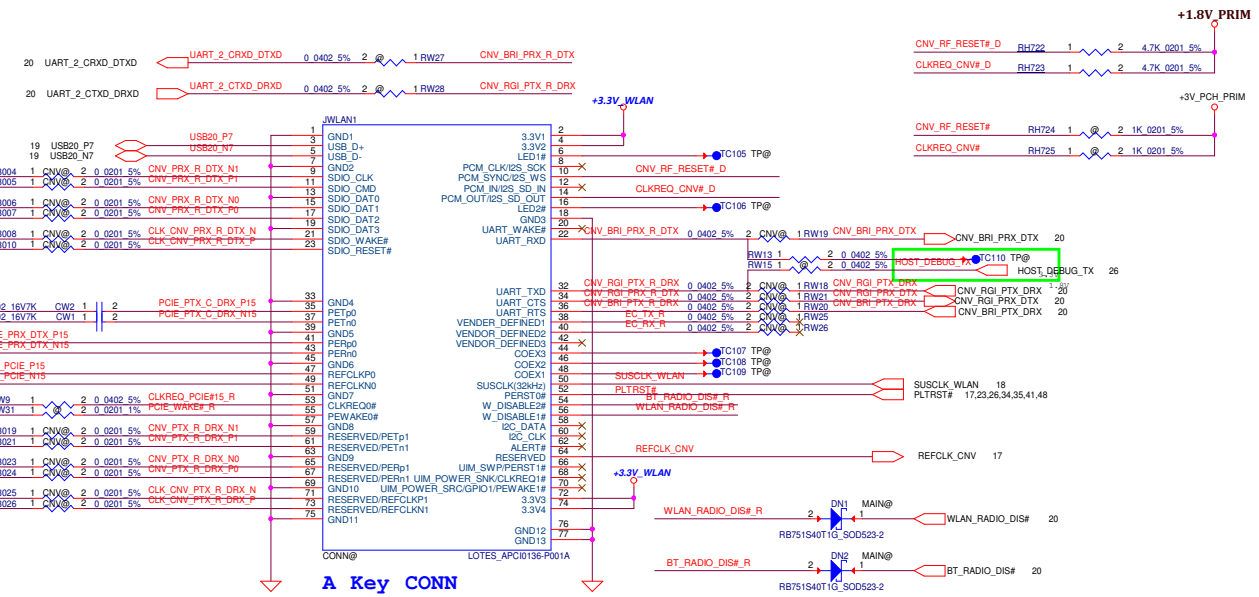
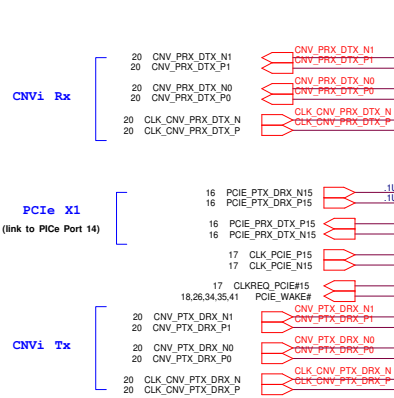
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVS LP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Act i vity	P11	

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				Sheet	20 of 78

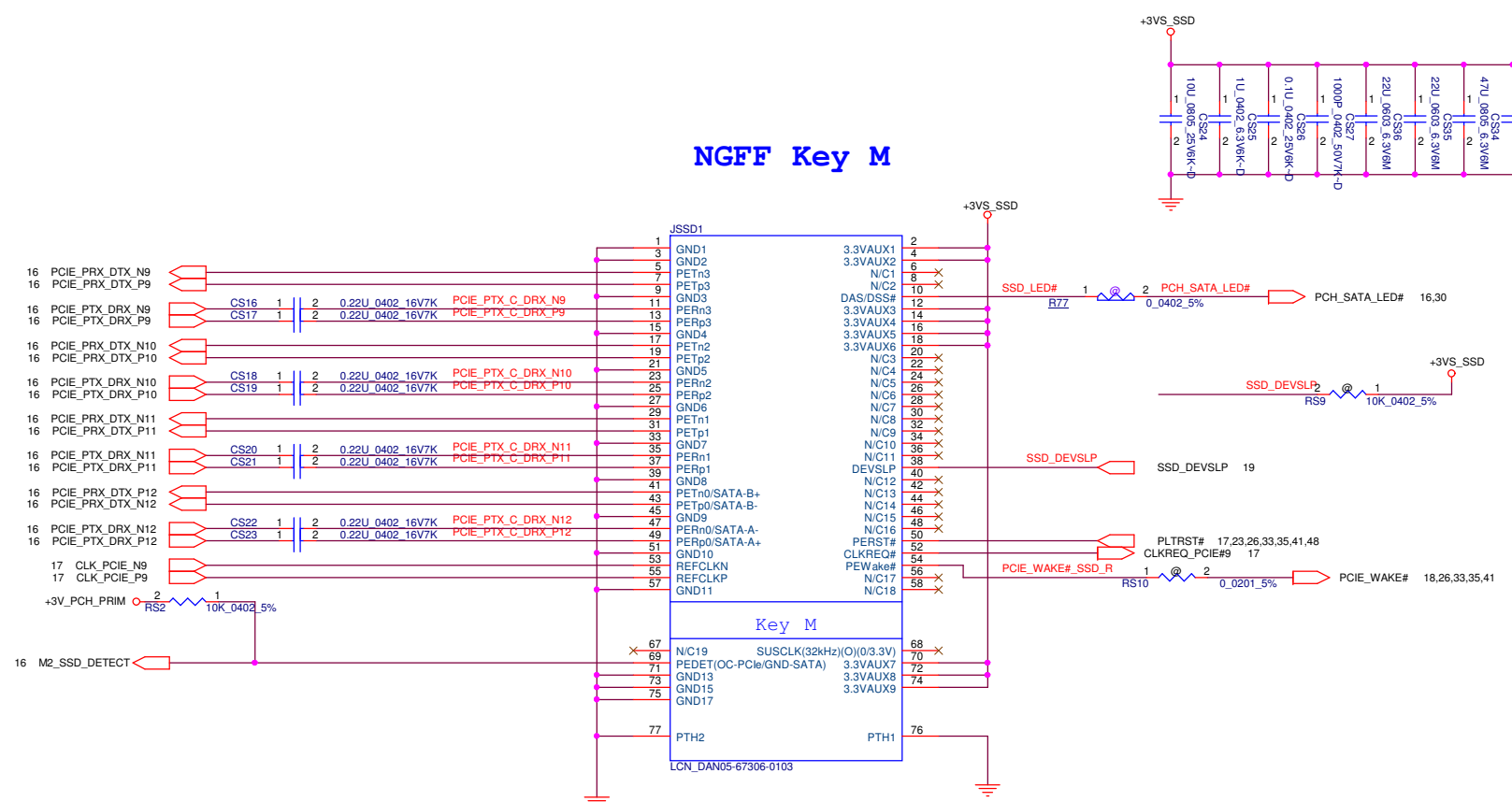
Main Func = WLAN / CNVi



Reserved for NGFF Debug Card

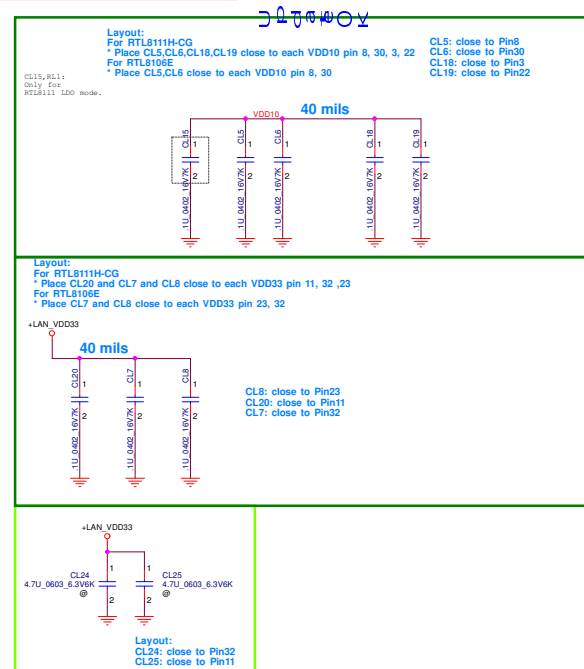


NGFF SSD

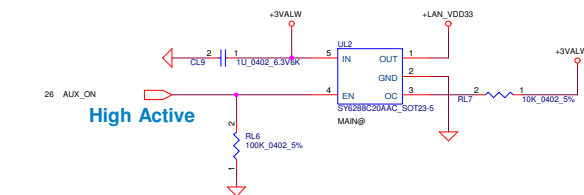


PEDET	Module Type
0	SATA
1	PCIe

Main Func = LAN

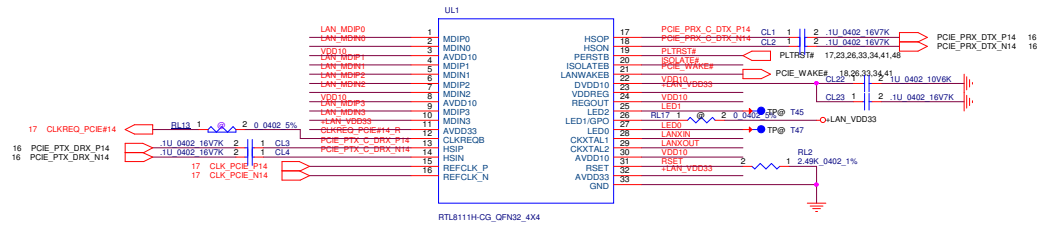
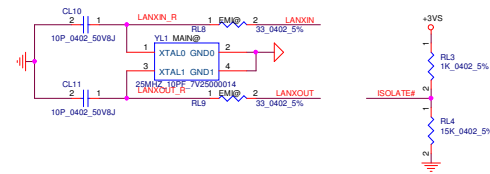


+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

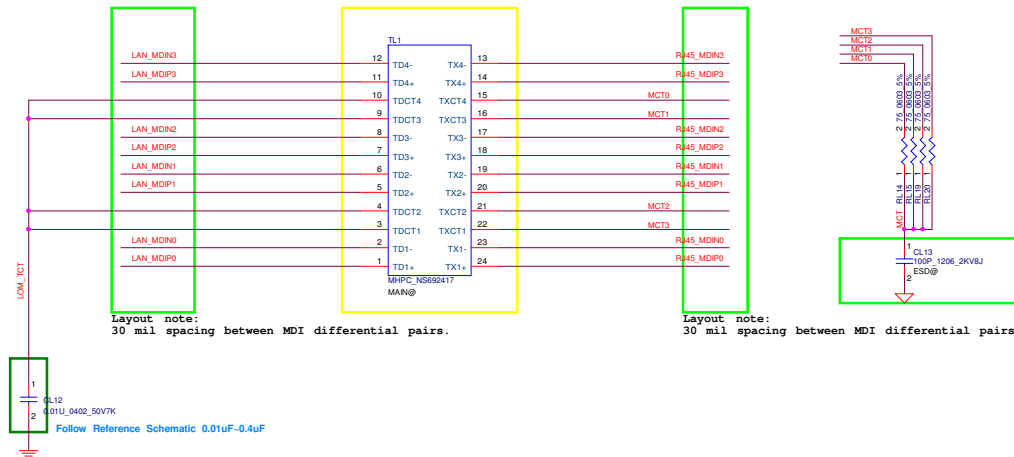


LAN Chip (10/100/1000M & 10/100M co-layout)

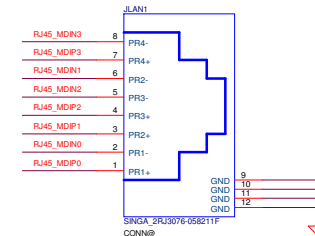
RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000045Y00
LDO mode	LDO mode
10/100/1000M	10/100M



LAN TransFormer (10/100/1000M & 10/100M co-layout)



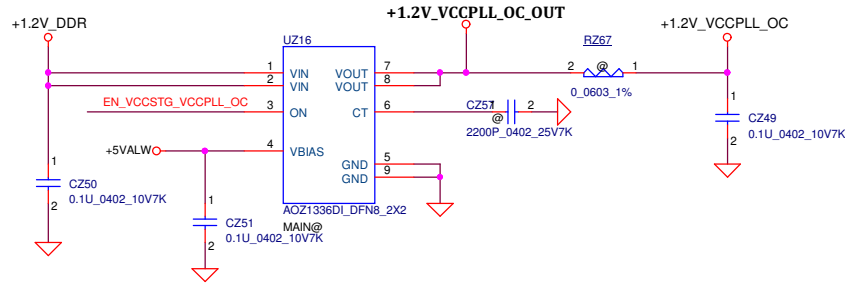
	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O



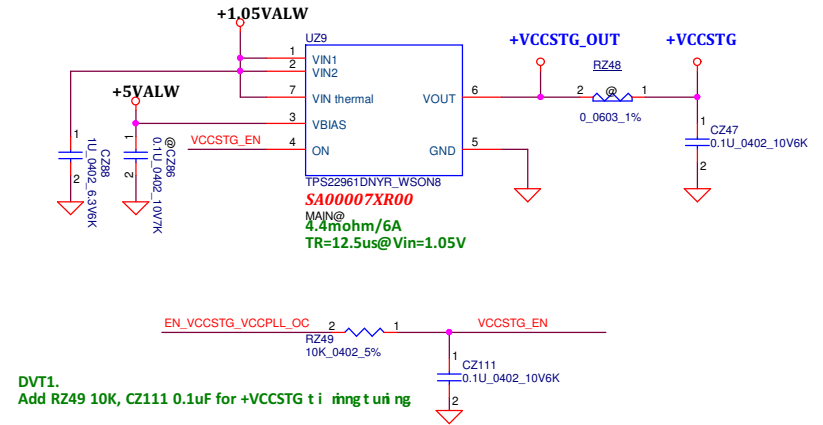
Main Func = DC/DC

+VCCPLL_OC Load Switch

H-Processor Line - Quad Core GT2
Max: 130 mA

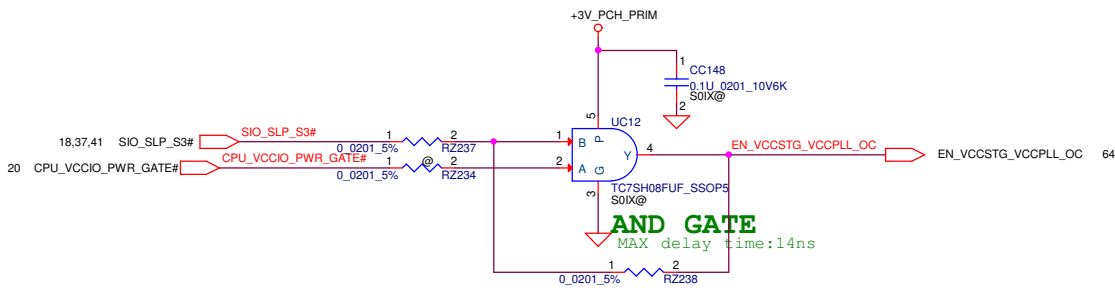


+VCCSTG Load Switch



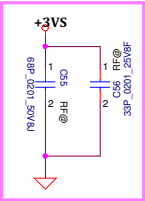
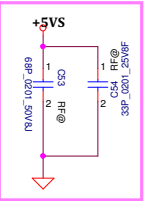
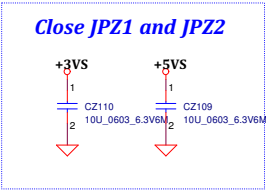
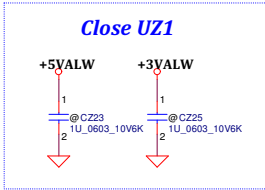
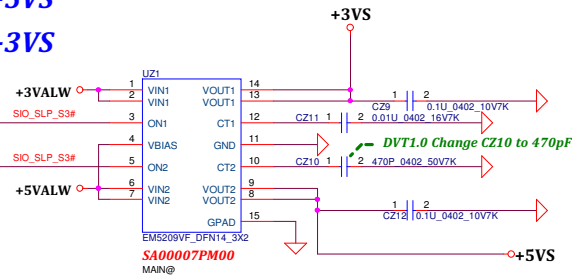
Power Gating by Modern Standby Control

+1.05VALW TO +1.0VS_VCCSTG

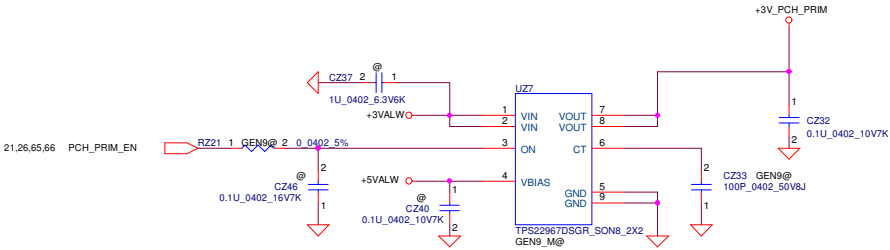


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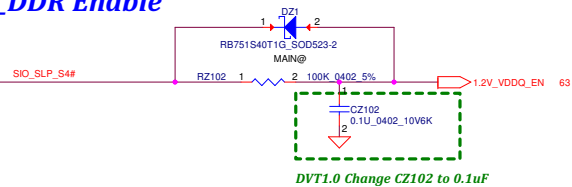
+5VALW to +5VS
+3VALW to +3VS



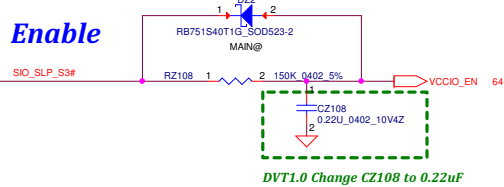
+3V_PCH_PRIM Load Switch



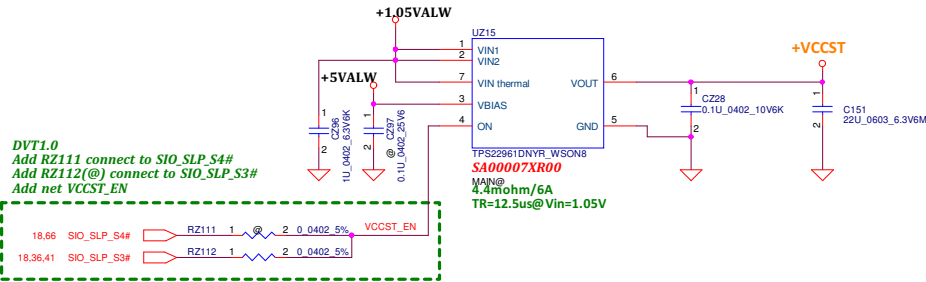
+1.2V_DDR Enable



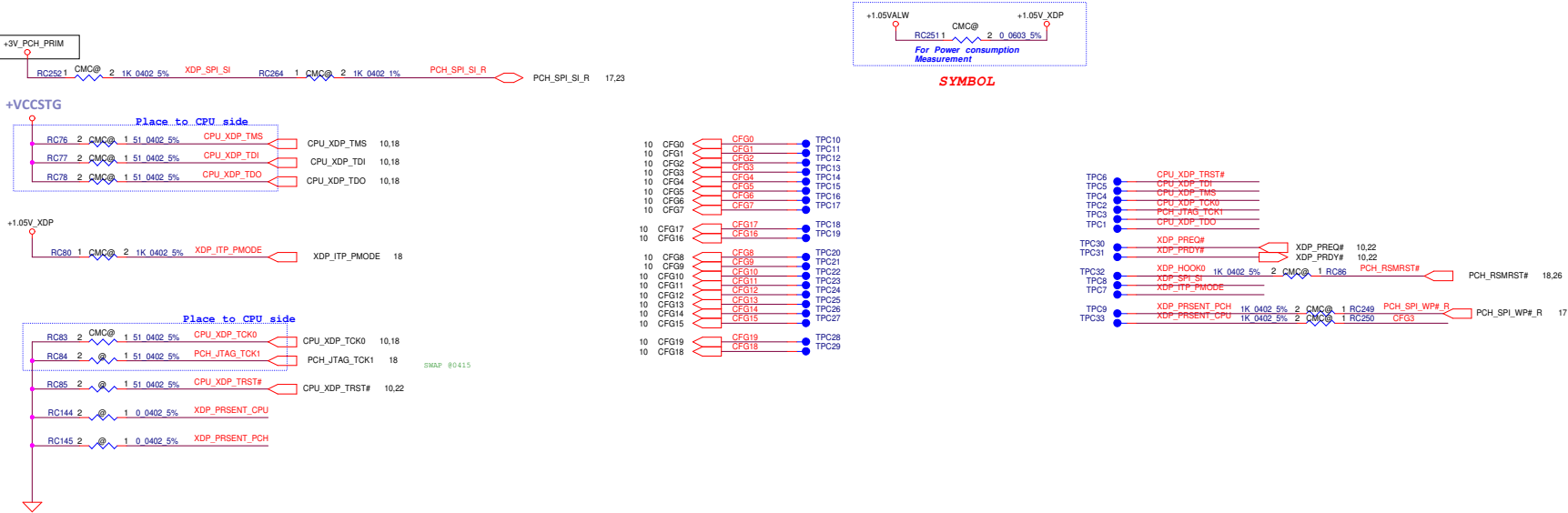
+VCCIO Enable



+VCCST Load Switch

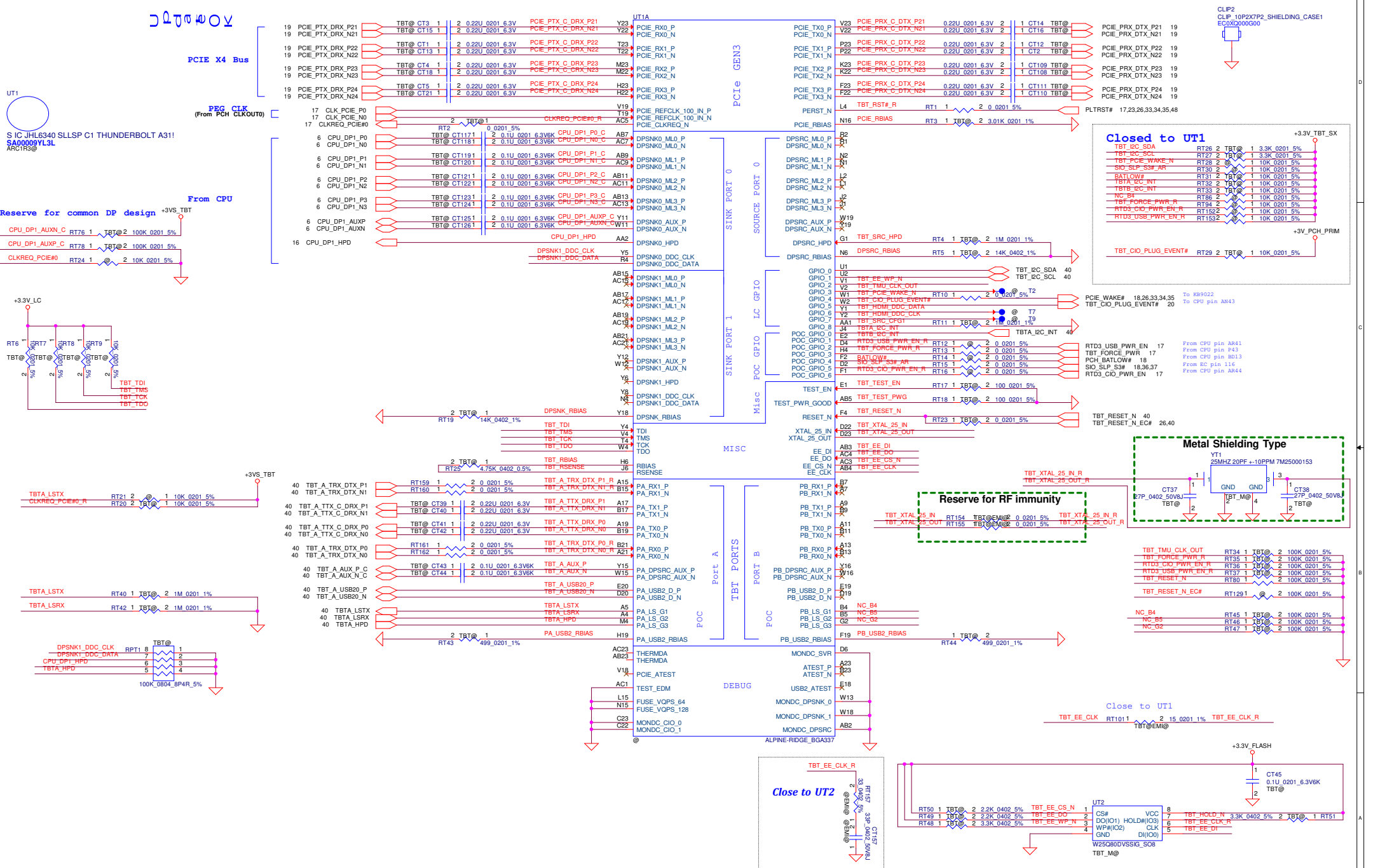


PRIMARY CMC CONN.



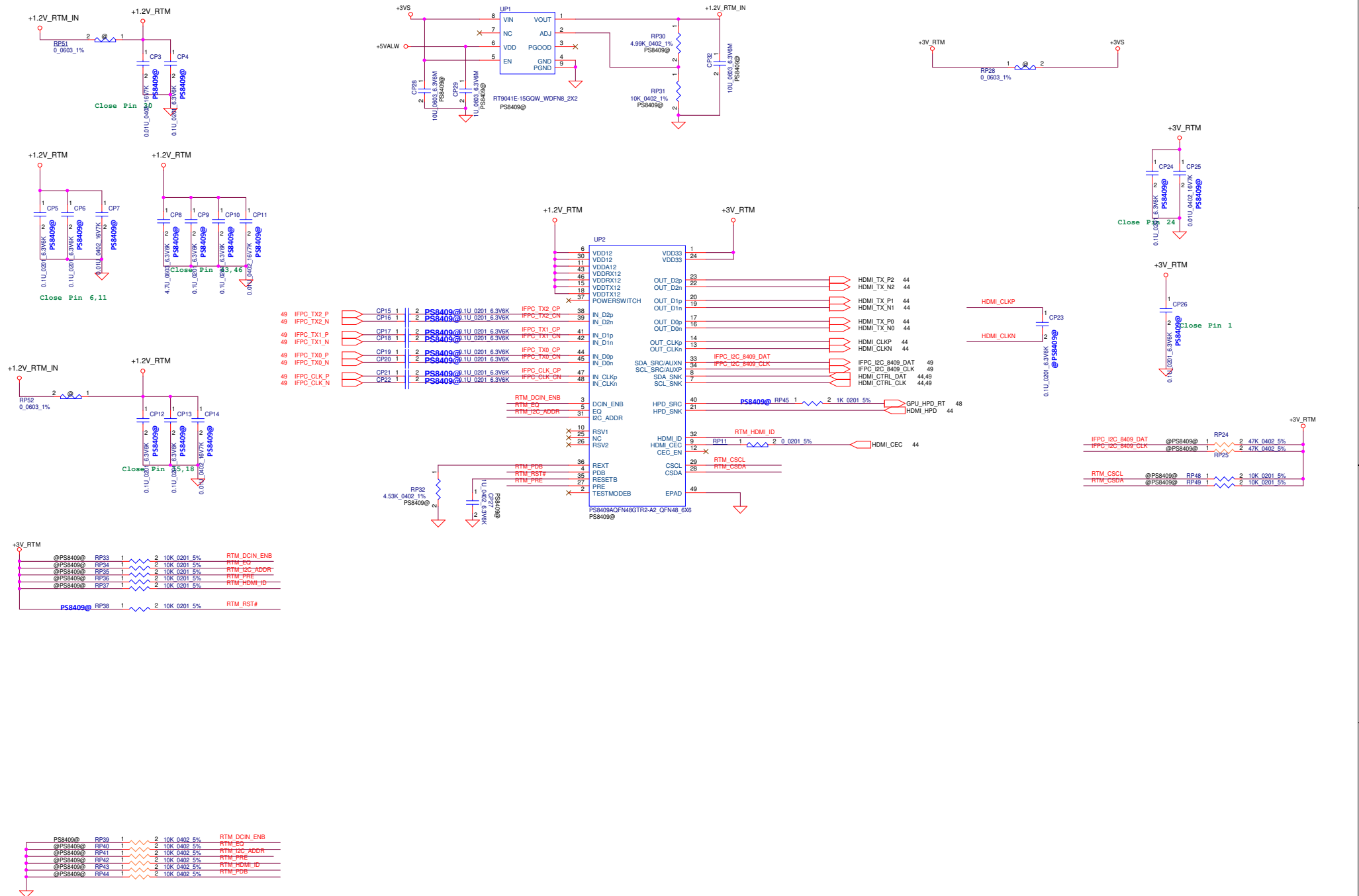
Reserved

Main Func = Thunderbolt



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				Date: Thursday, March 22, 2016	Sheet 41 of 78	

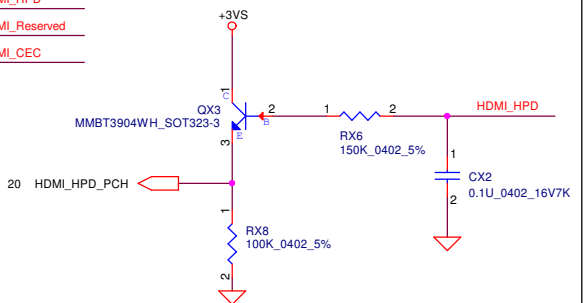
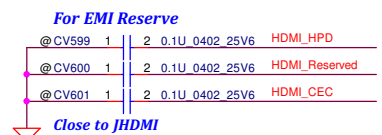
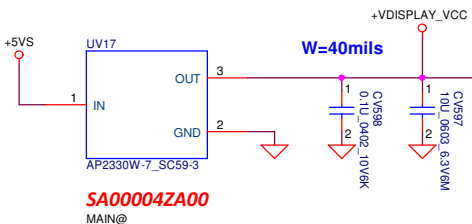
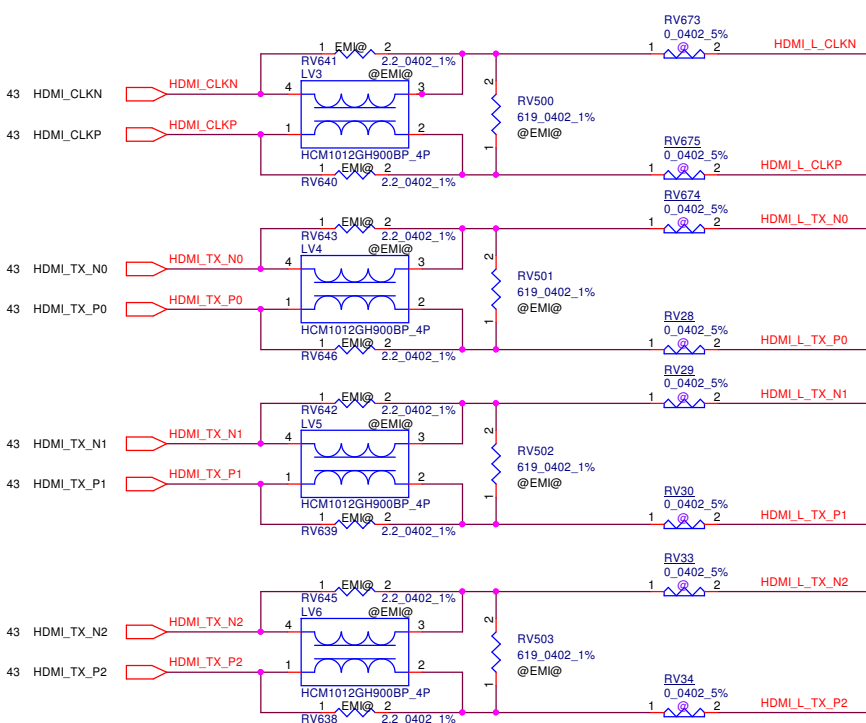
Main Func = Retimer



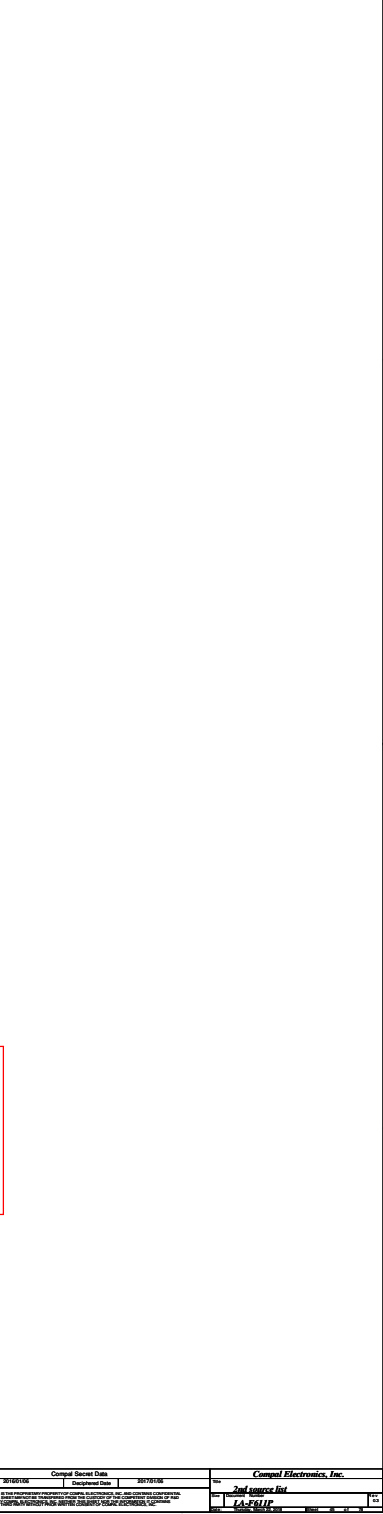
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Date: Thursday, March 22, 2018		Sheet		43 of 78	
0.3					

Main Func = HDMI

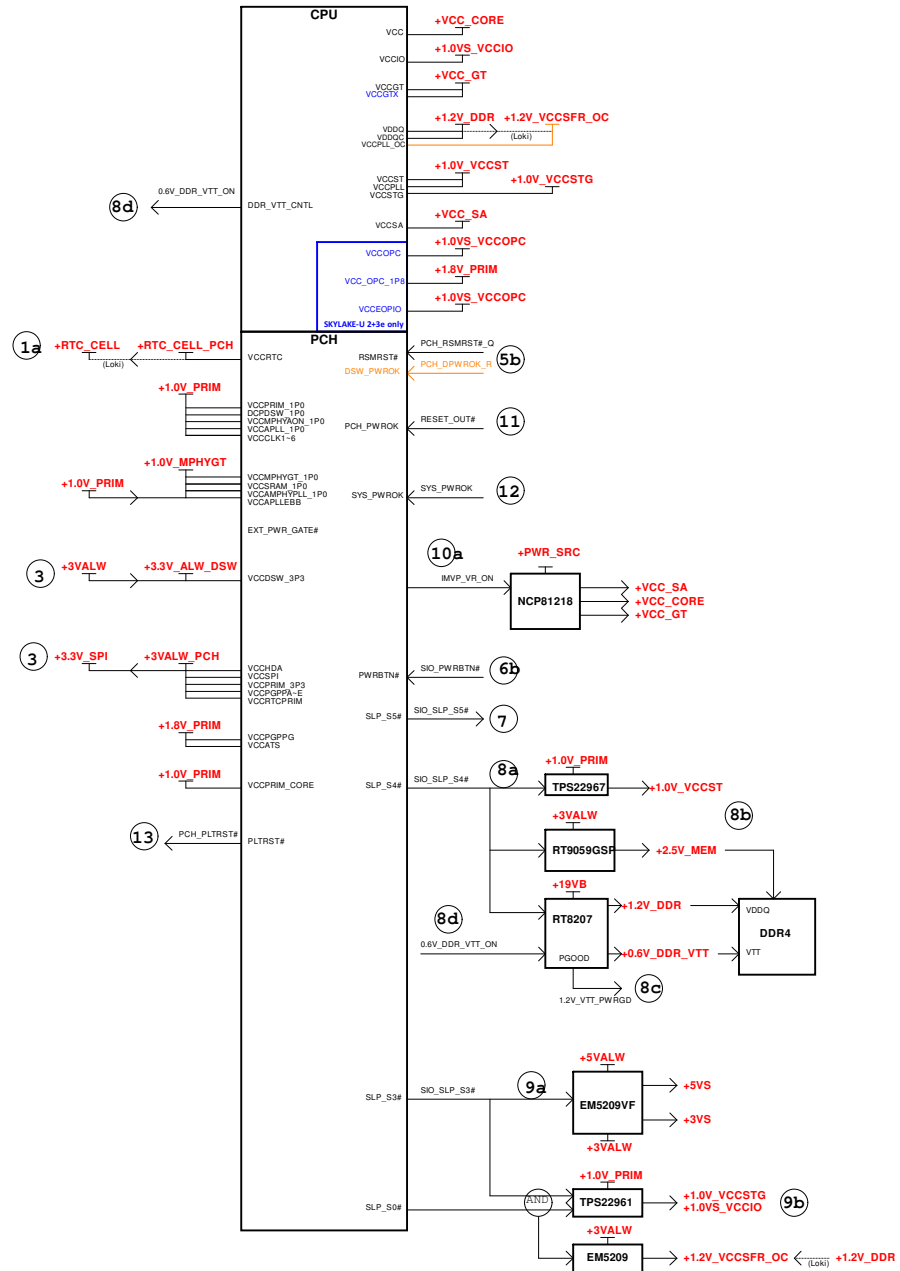
Place close to JHDMI1




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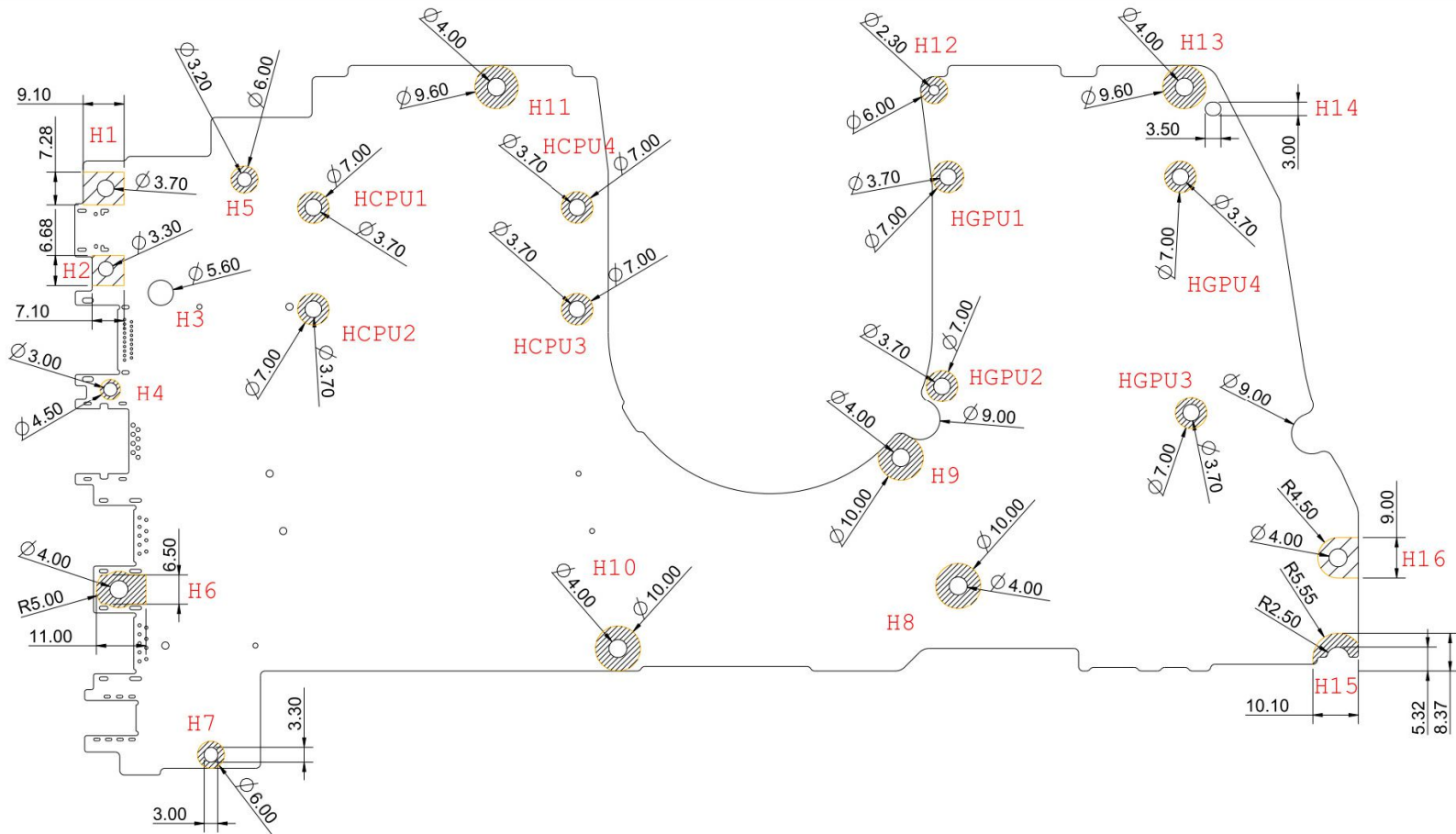
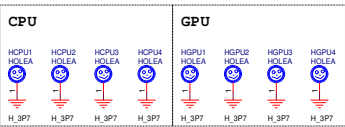
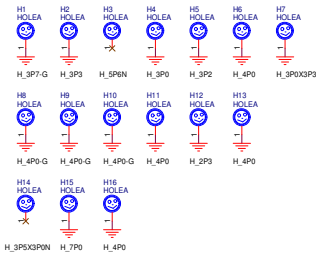
Block diagram of the power management system for the EC1416. The diagram shows the EC1416 chip connected to various power components. On the left, inputs include a Power Button (6a), PRIM_PWRGD (4), SIO_PWRBTN# (6b), RUN/PWROK and ALL_SYS_PWRGD (10b), RESET_OUT# (11), and SYS_PWRROK (12). On the right, outputs include EN_5V (2) to SY8180 (VL, +5VALW), EN_3V (2) to SY8286 (+3VLP, +3VALW), POK signals to RT6228 (+1.0V_PRIM) and RT8061 (+1.8V_PRIM), SIO_SLP_SUS# (2a) to EM5209 (+3VALW_PCH), and PCH_RSMRST# (5a).



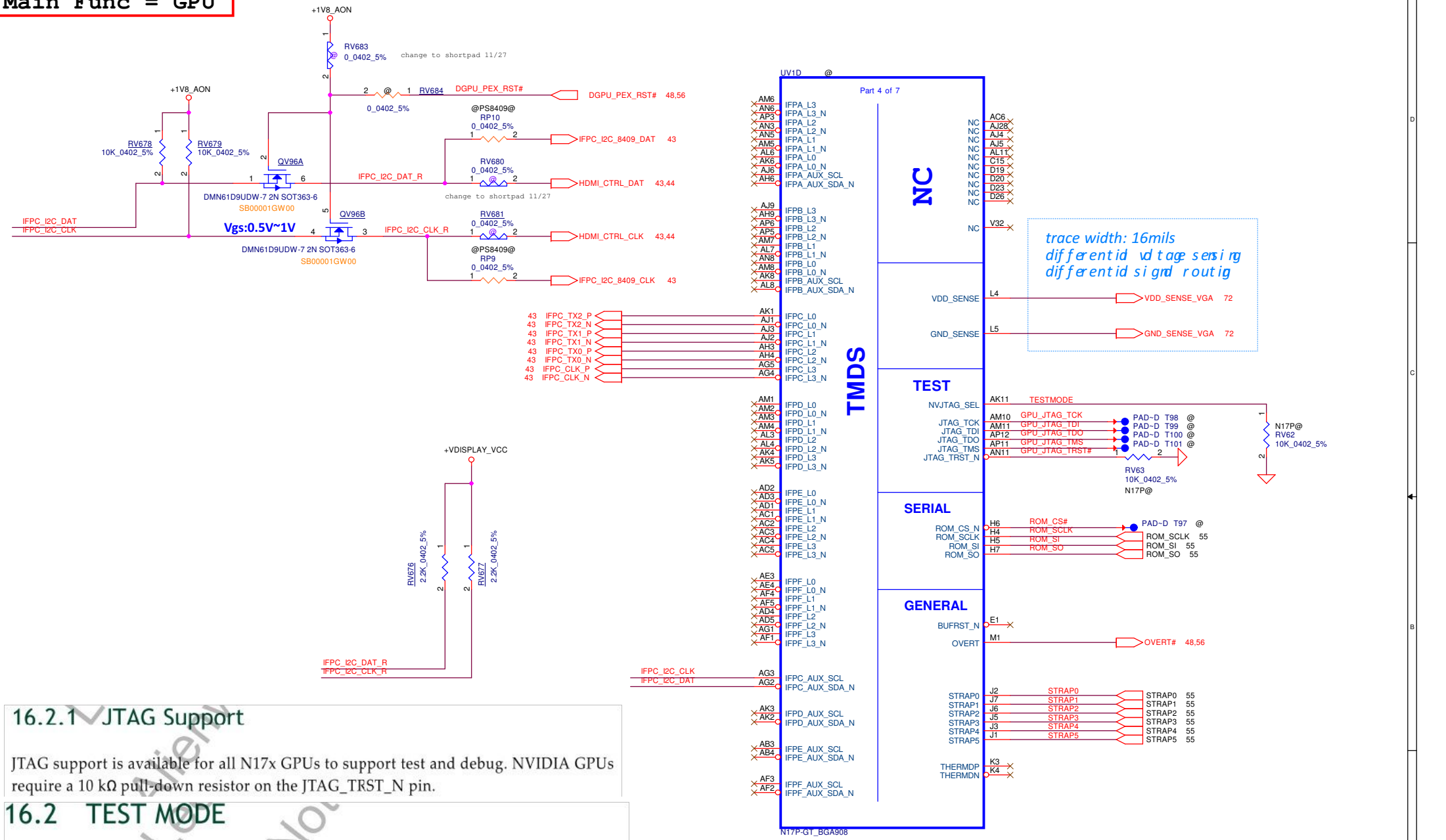
Security Classification	Compul Secret Data			
Issued Date	2016/01/06	Deciphered Date	2017/10/06	Title POWER SEQUENCE Doc No FA-F611P Date Deciphered 08/28/2018
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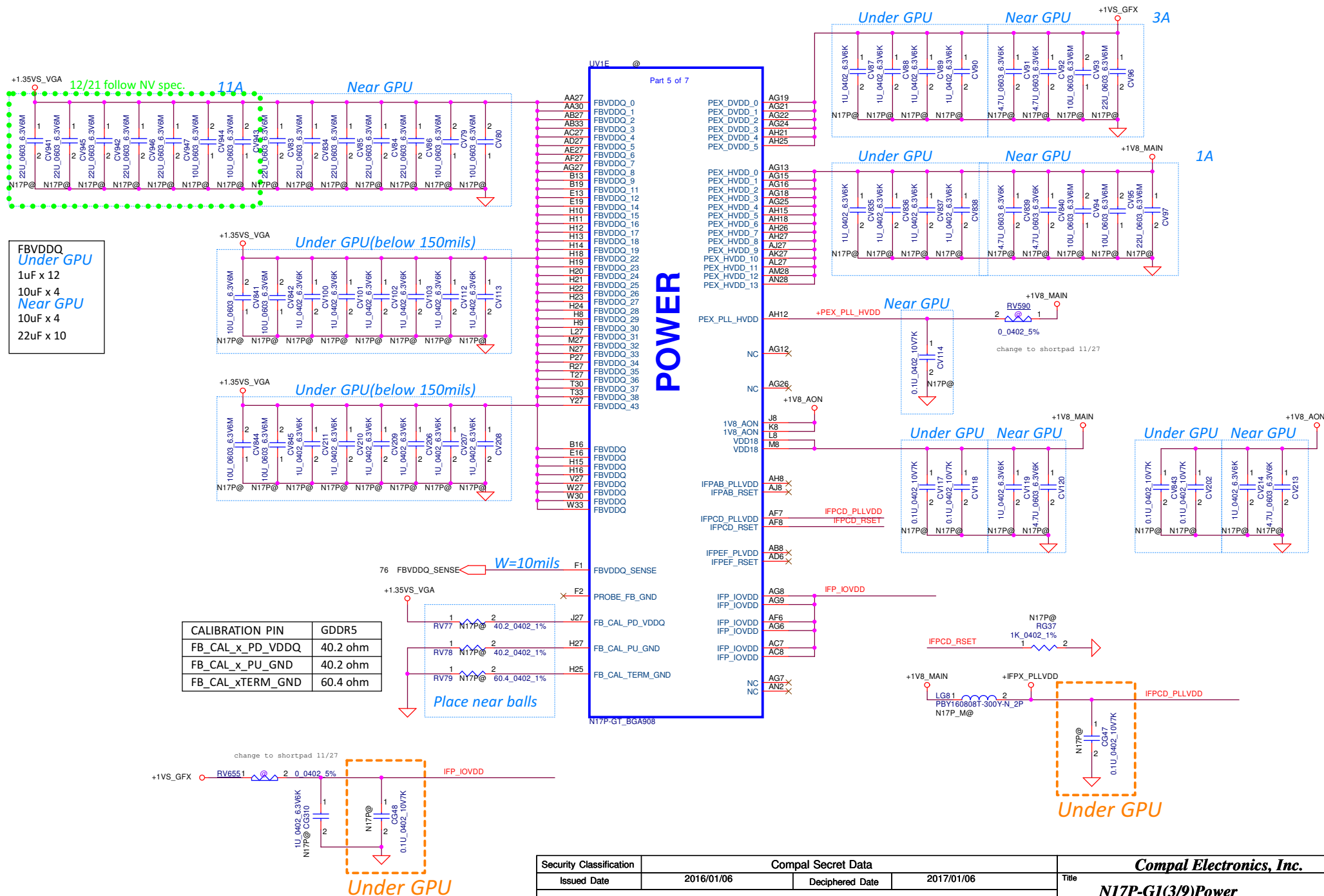
Screw hole/FD



Main Func = GPU



Main Func = GPU



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Main Func = GPU

POWER

GND

Security Classification

Issued Date	Deciphered Date	2017/01/06
2016/01/06		

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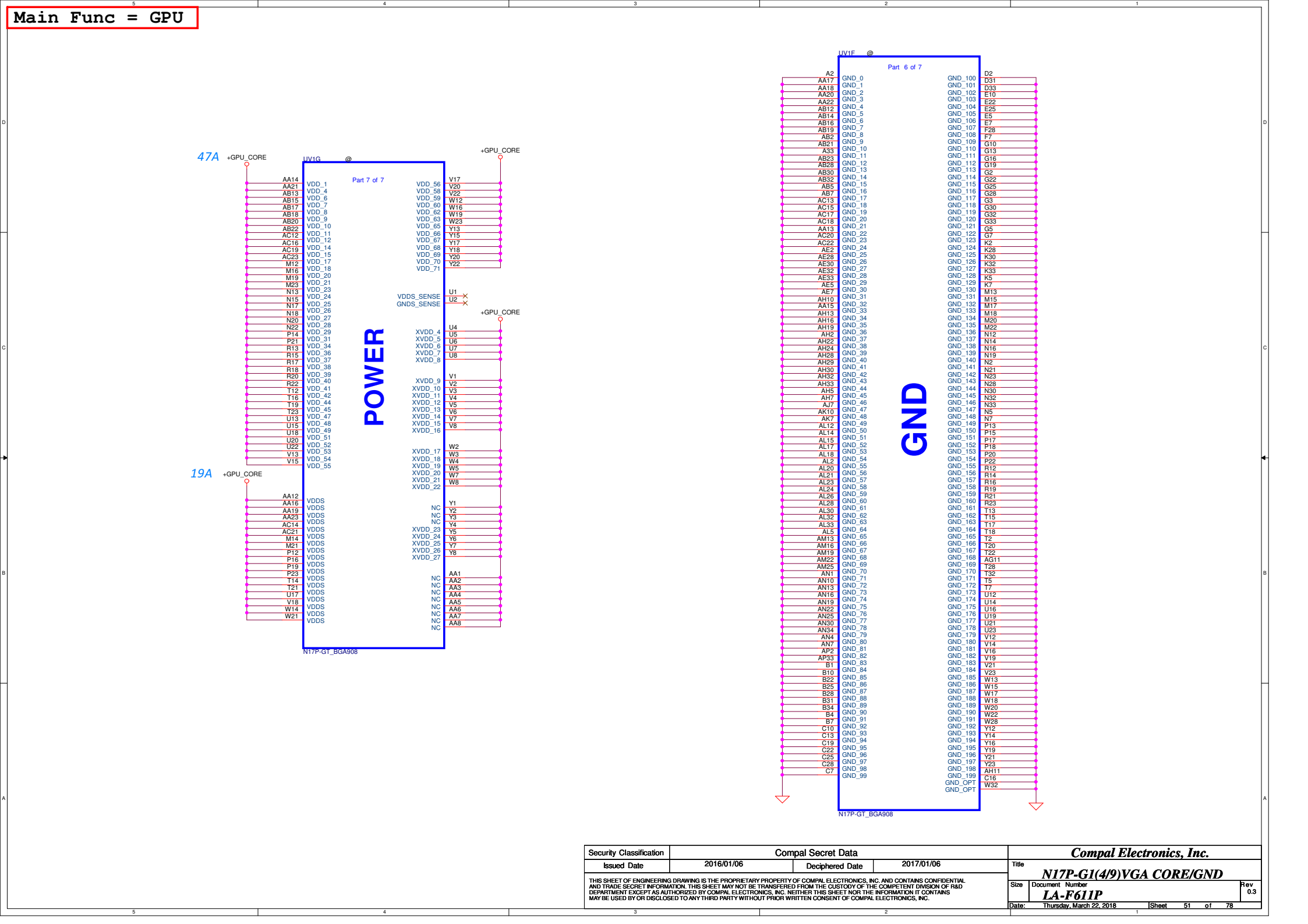
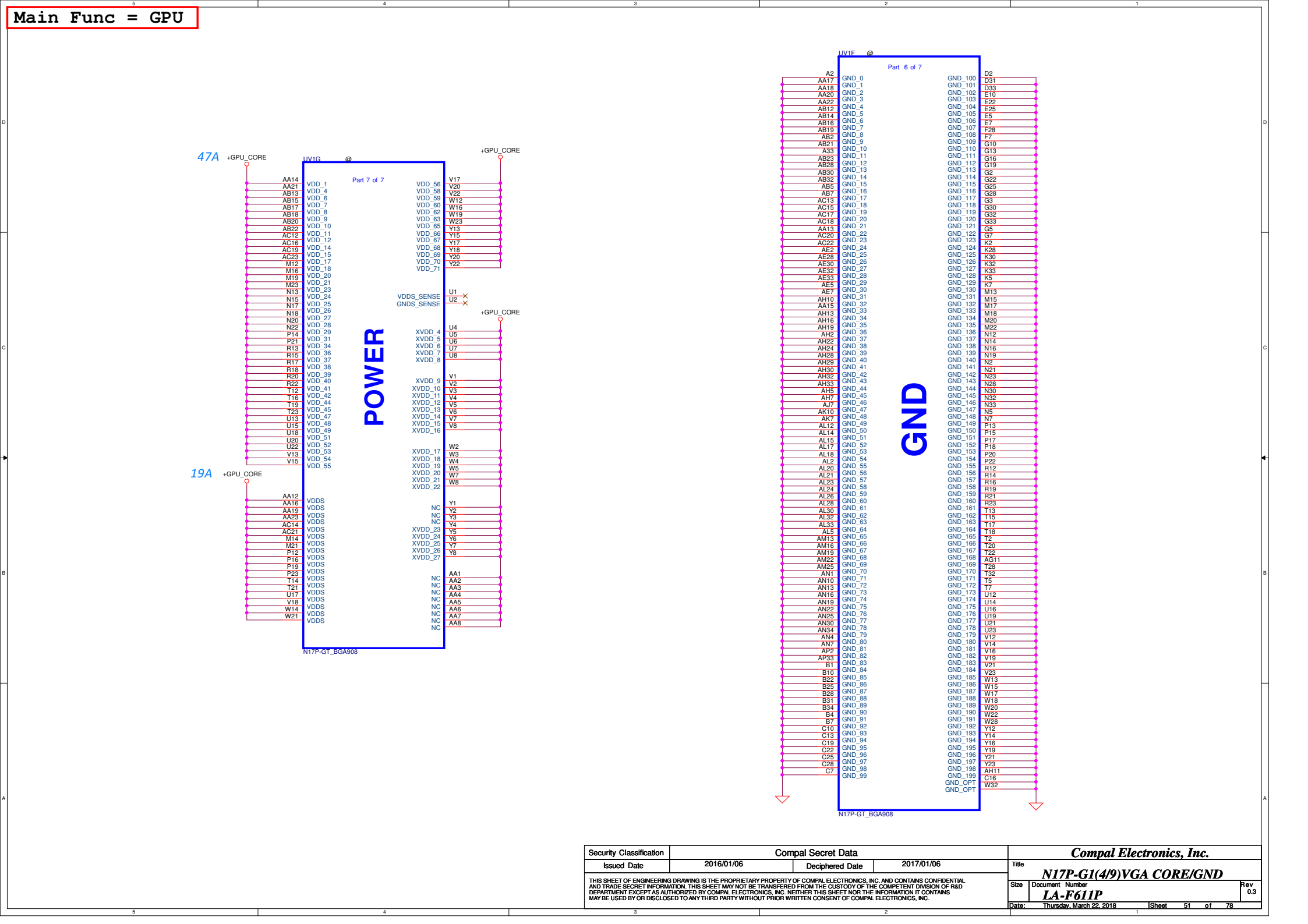
Title

N17P-G1(4/9)VGA CORE/GND

Size **Document Number** **Rev**

LA-F611P **0.3**

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Main Func = GPU

47A +GPU_CORE

19A +GPU_CORE

POWER

GND

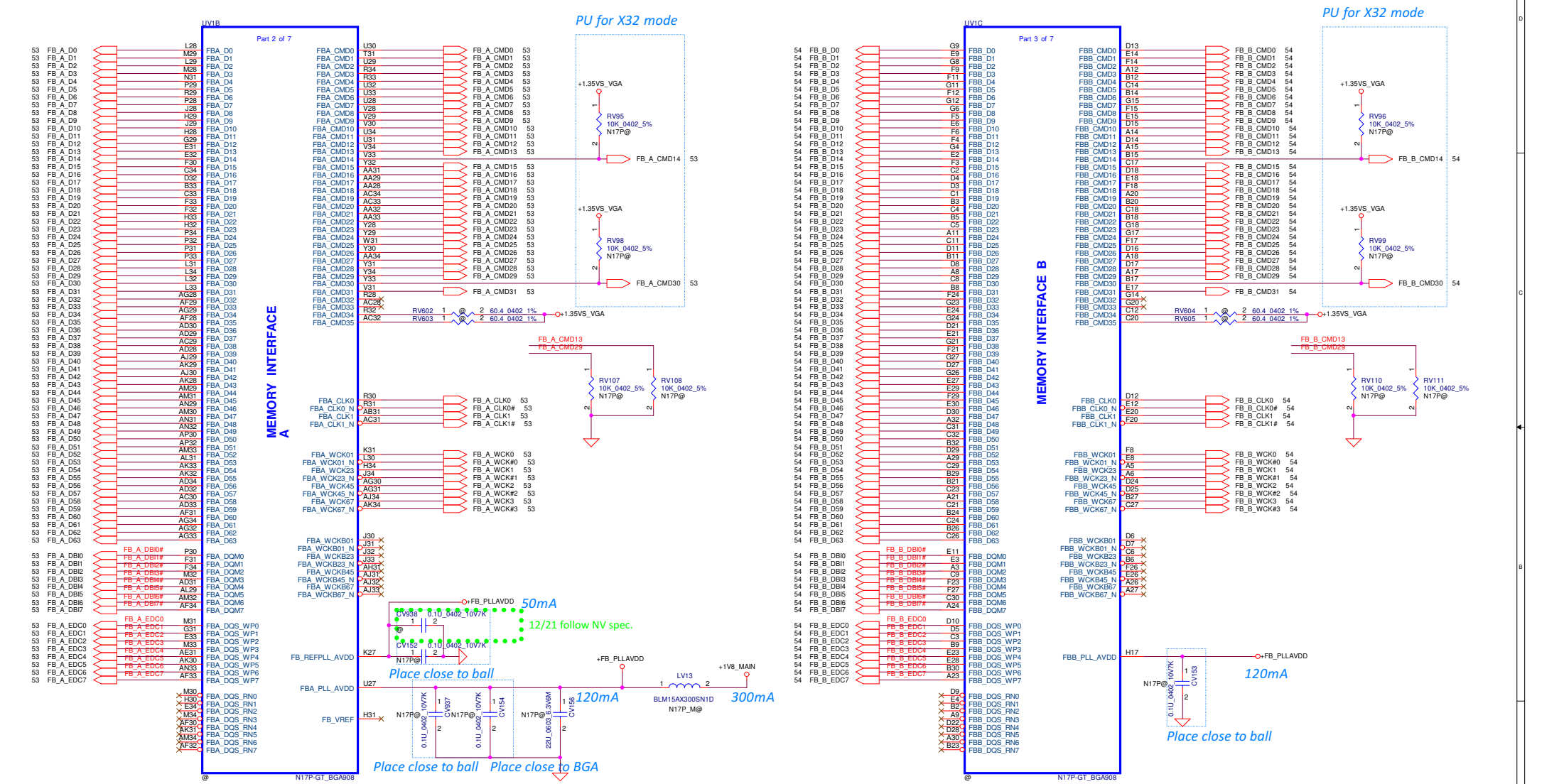
Part 7 of 7

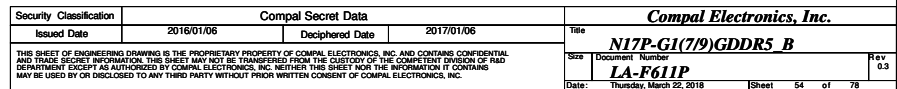
Part 6 of 7

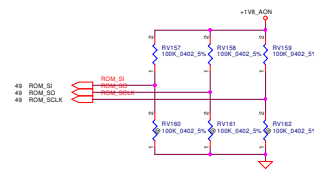
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Main Func = GPU







+1.8V_AON

R1 100K

strap pin

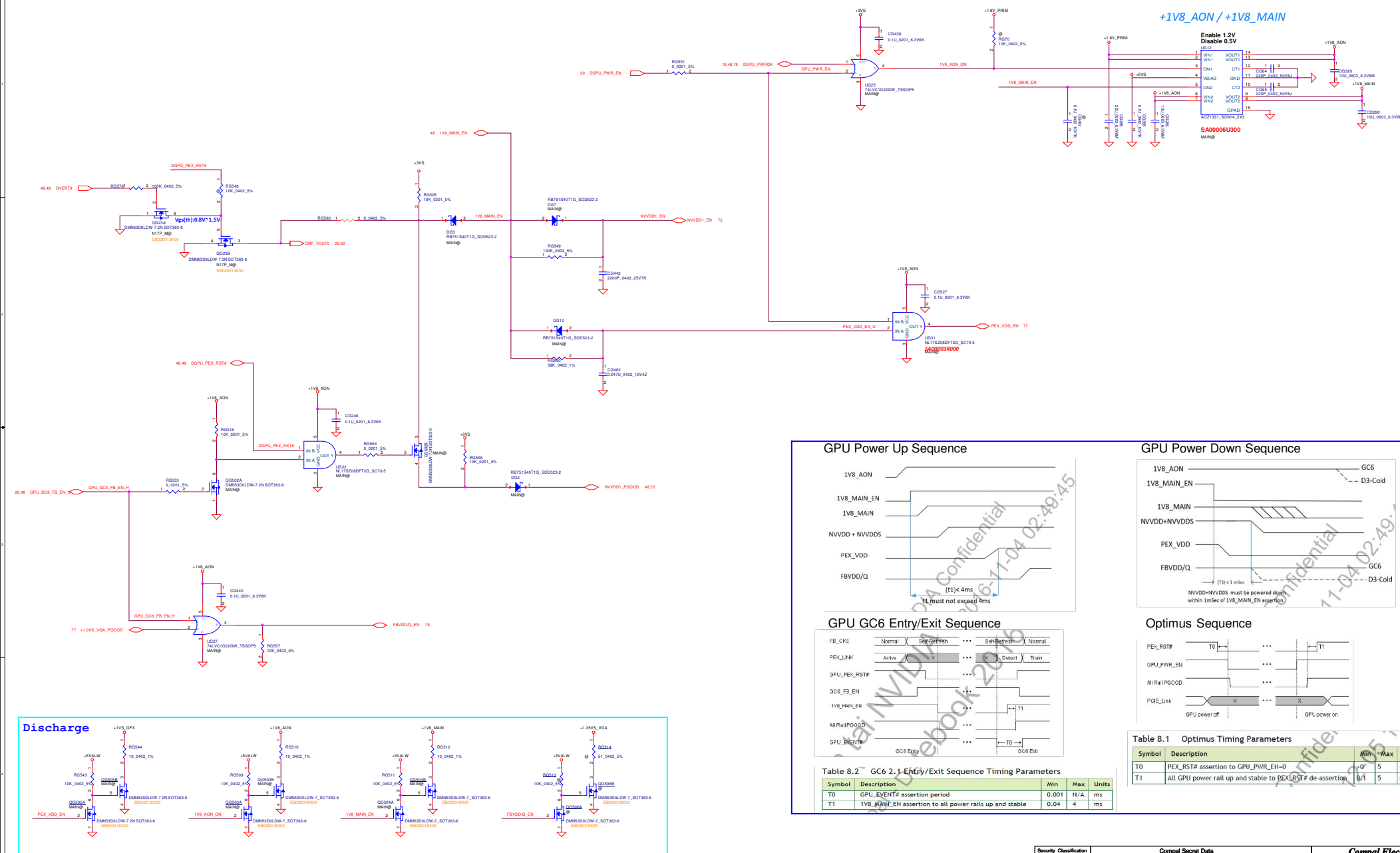
R2 100K

GPU config

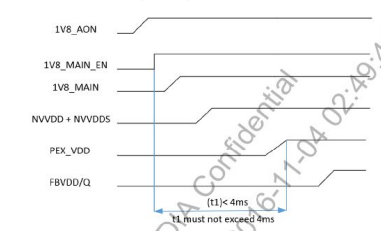
L: stuffed R1 only
L: stuffed R2 only
M: stuffed R1 and R2

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU
DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID
VGA_DEVICE	
Low	3D Device
High	VGA Device
PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

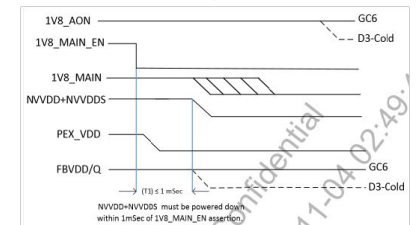
Discharge



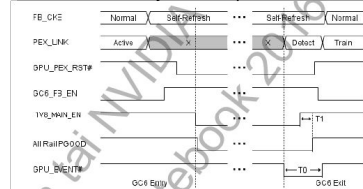
GPU Power Up Sequence



GPU Power Down Sequence



GPU GC6 Entry/Exit Sequence



Optimus Sequence

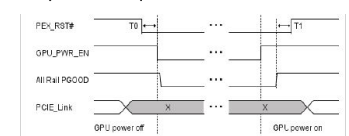


Table 8.1 Optimus Timing Parameters

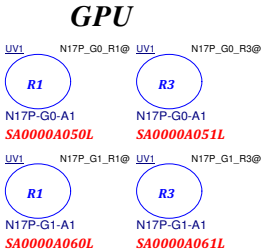
Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

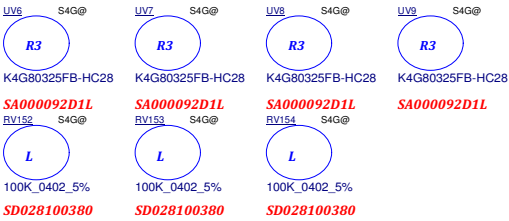
Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

MODEL NAME : CALXX/CALXX
PCB NO : LA-F611P

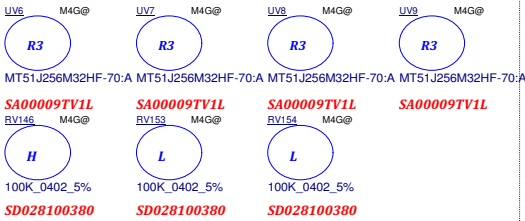
Bom
Structure



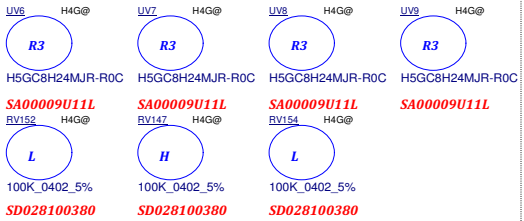
X76 : S4G@ X76XXXXXLXX
Samsung 4G



X76 : M4G@ X76XXXXXLXX
Micron 4G



X76 : H4G@ X76XXXXXLXX
Hynix 4G



Samsung 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
0	L	L	L

Micron 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
1	L	L	H

Hynix 4G

Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
2	L	H	L

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V ¹	Samsung	K4G80325FB-HC28	B-die	0x0	Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	Gbps	N/A	N/A	Substitution allowed with waiver ¹
			Micron	MT51J256M32HF-70-A	A-die	0x1	Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80-A	A-die	0x1	Gbps	N/A	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24MJR-R4C	M-die	0x2	Gbps	N/A	N/A	Substitution allowed with waiver ¹
4 Gb	128Mx32	1.35V and 1.5V ¹	Samsung	K4G41325FE-HC28	E-die	0x7	Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	Gbps	N/A	N/A	Substitution allowed with waiver ¹
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	Gbps	N/A	Full	Production ready
			Hynix	H5GC4H24AJR-R4C	A-die	0x6	Gbps	N/A	N/A	Substitution allowed with waiver ¹
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
			Micron	EDW4032BABG-70-F	A-die	0x8	Gbps	N/A	Full	Post production ready

[illegible]

Adapter protection
if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

Battery protection
asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW_PROCHOT# is issued by EC

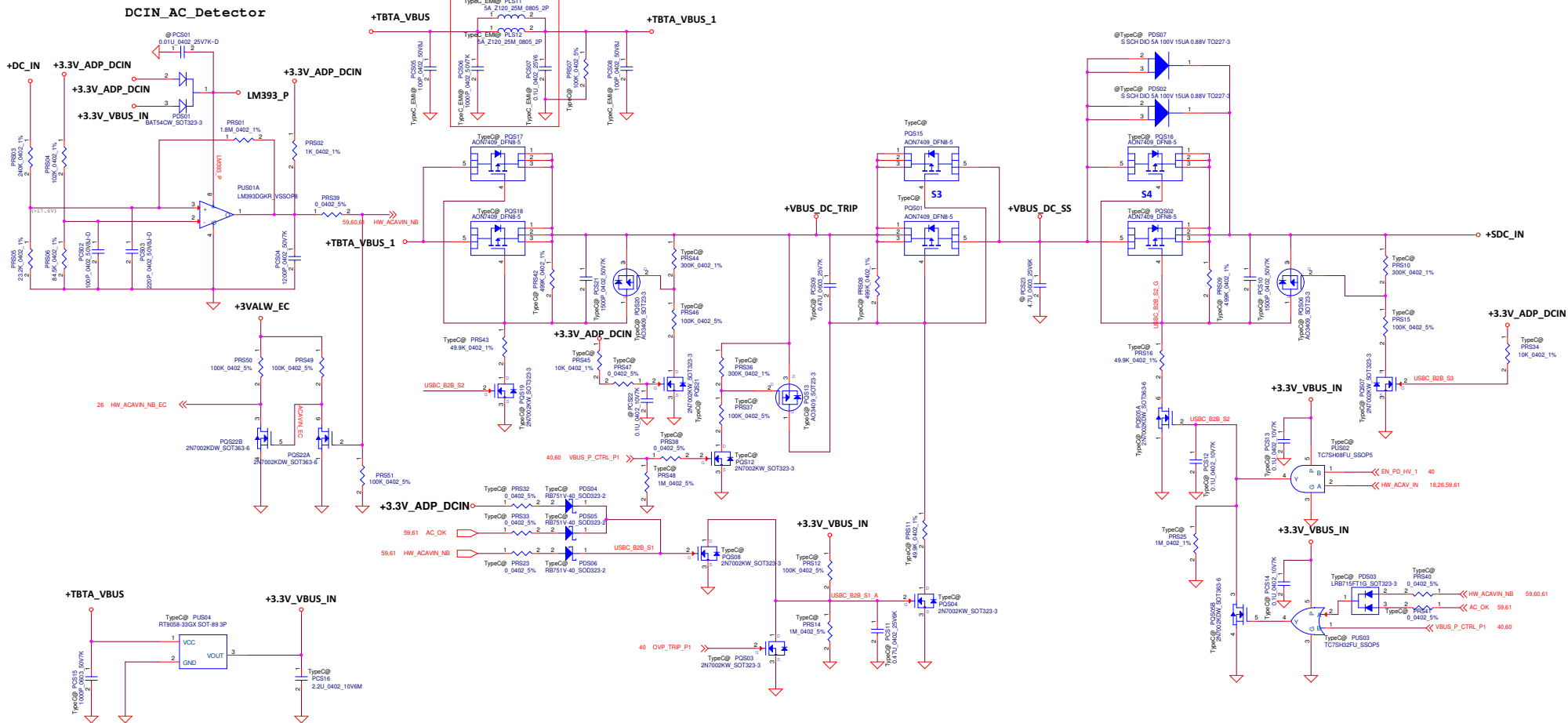
Erp lot6 Circuit

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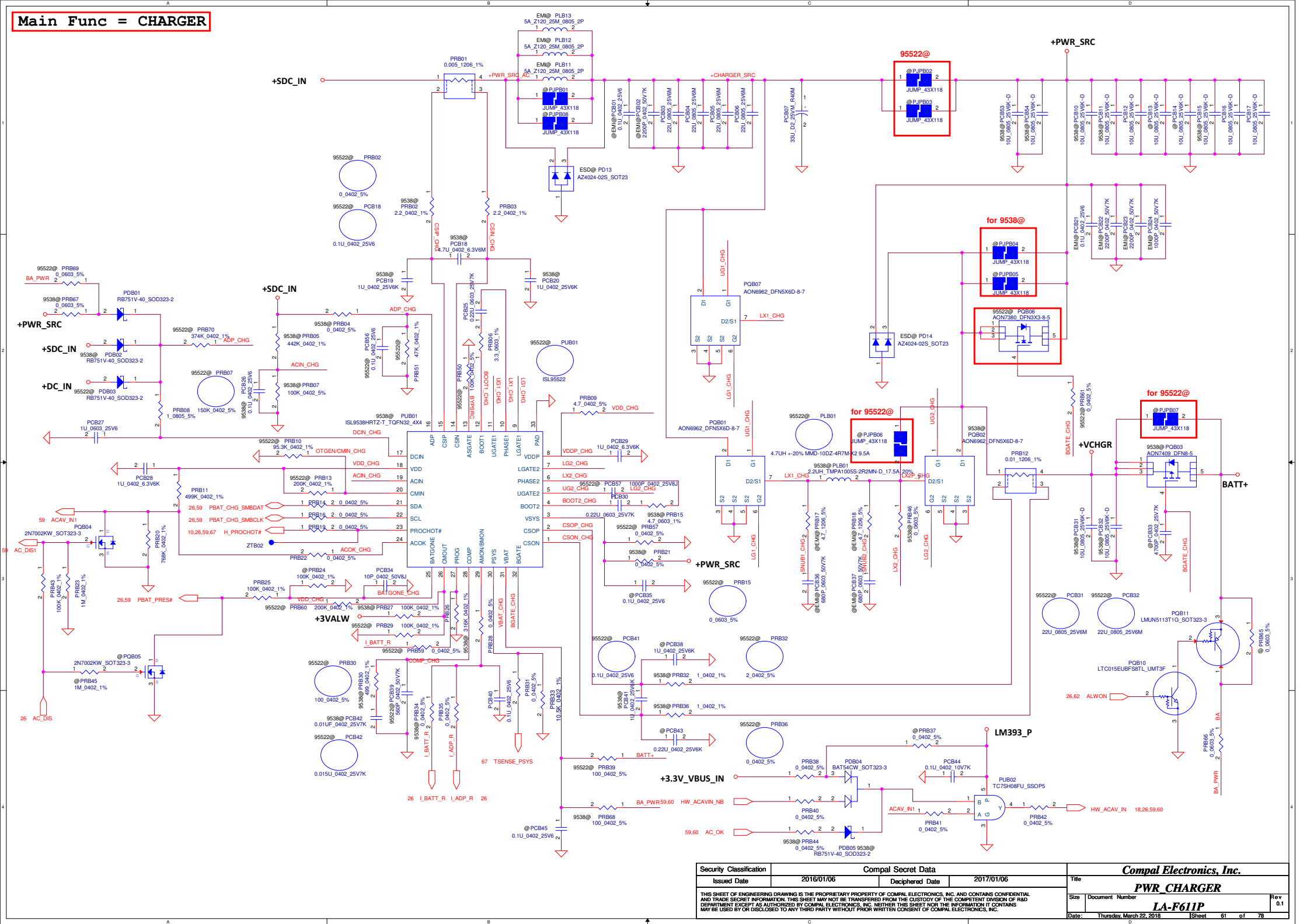
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Main Func = Type-C PD Selector

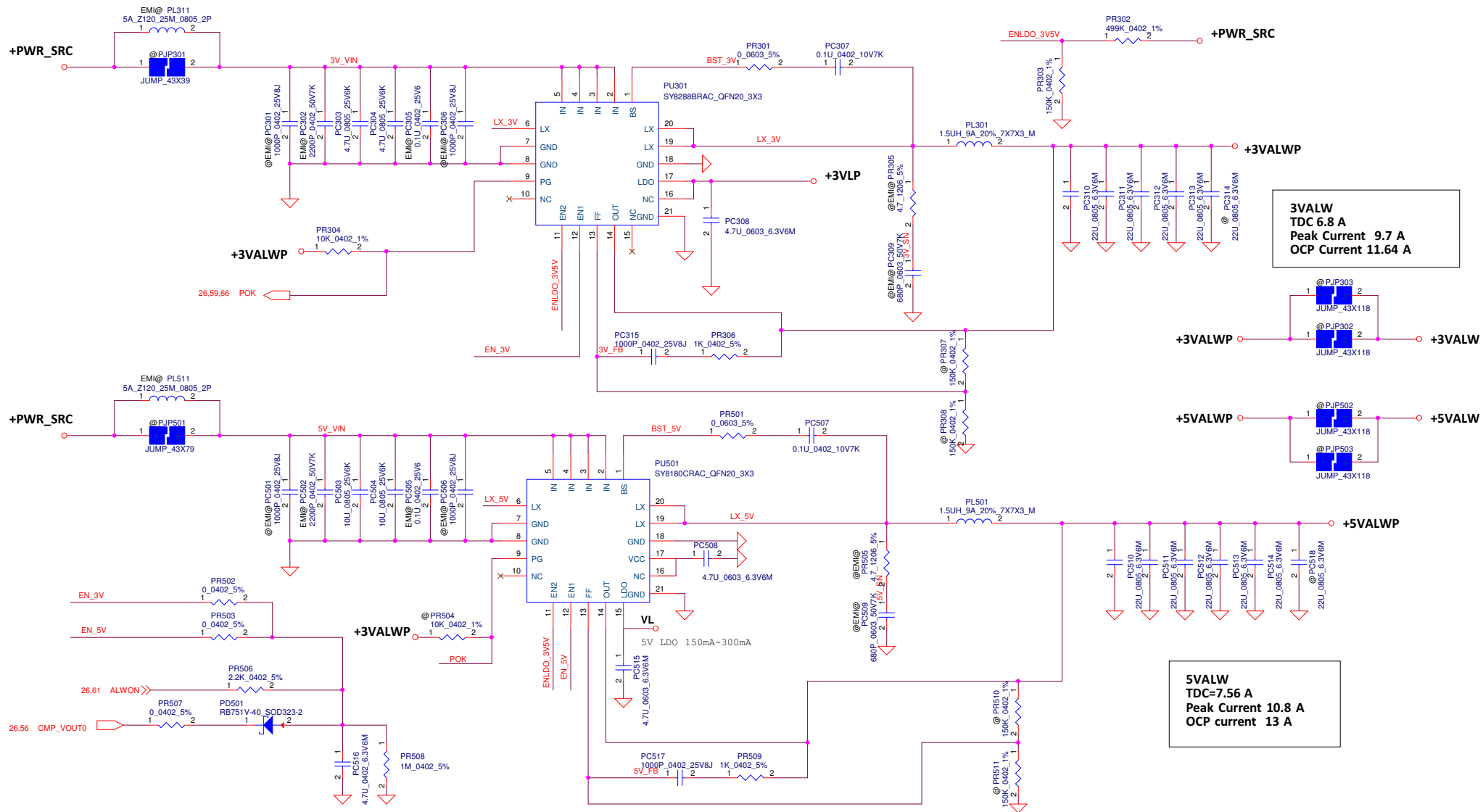


Main Func = CHARGER



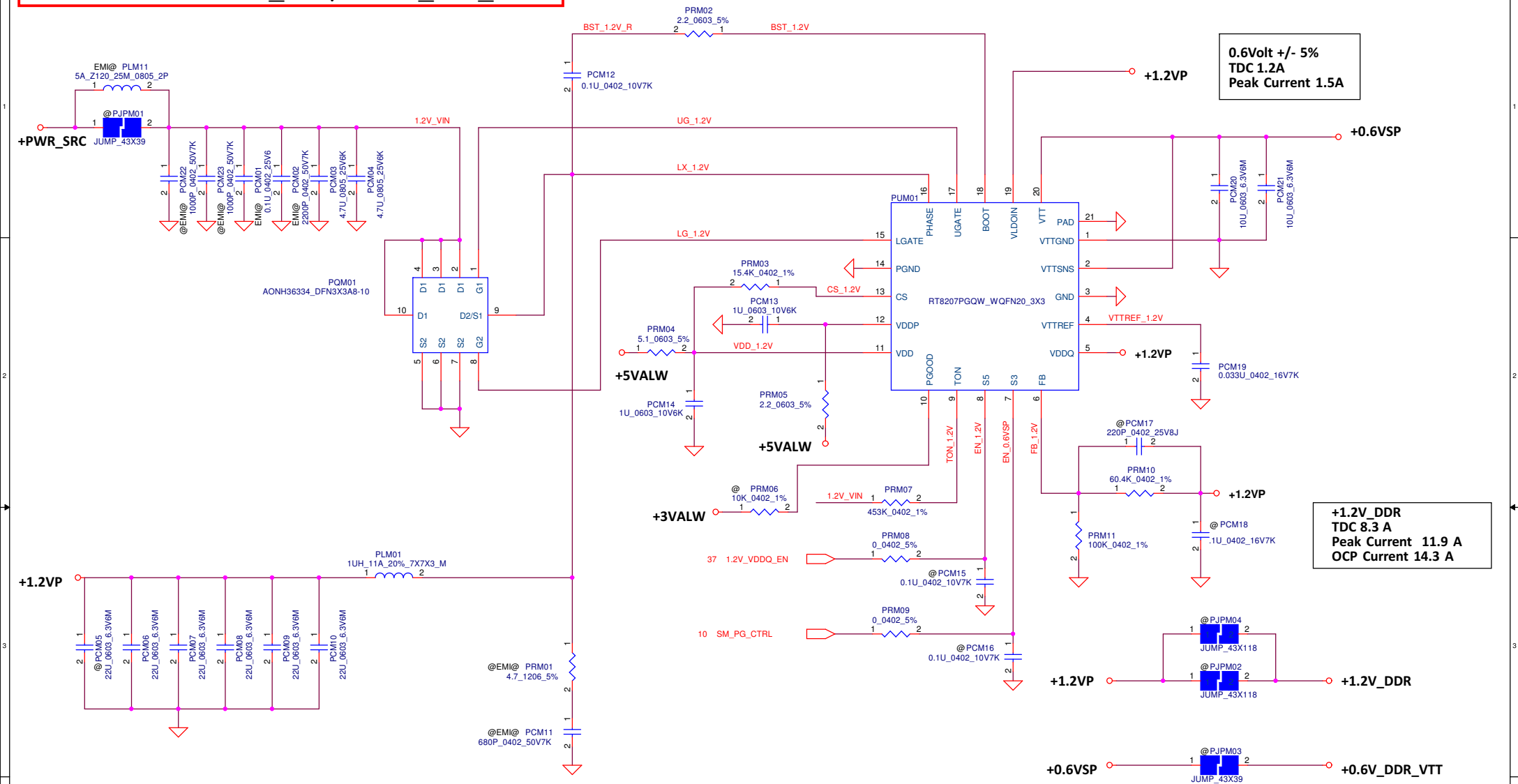
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Main Func = 3.3VALW/5VALW



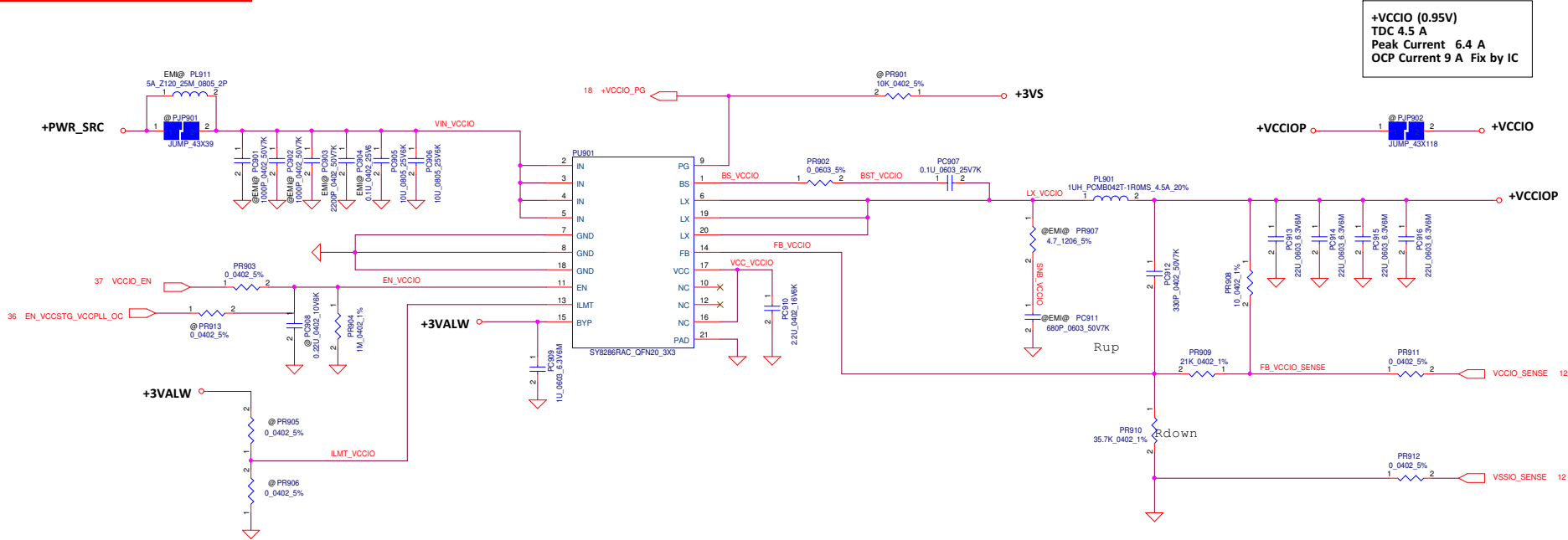
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Main Func = 1.2V_DDR/+0.6V_DDR_VTT



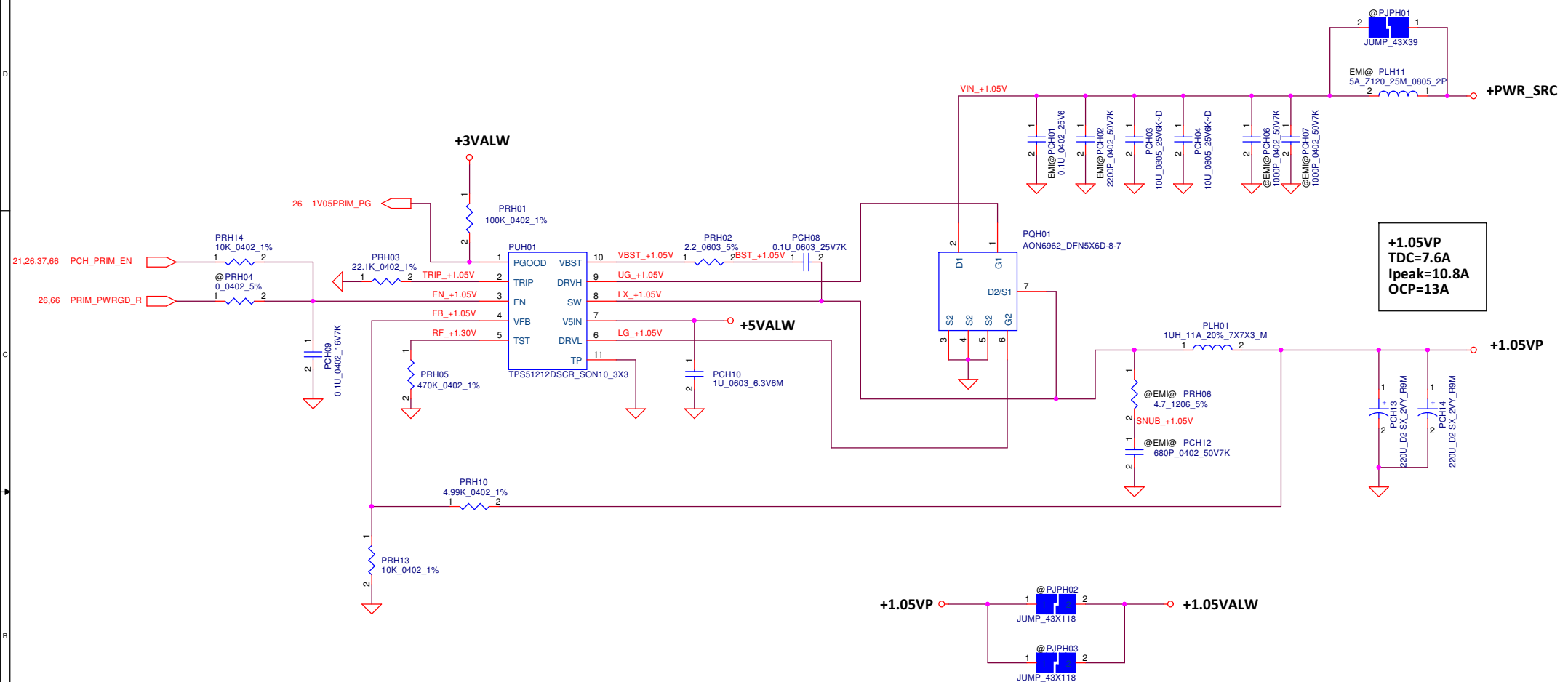
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Main Func = VCCIO



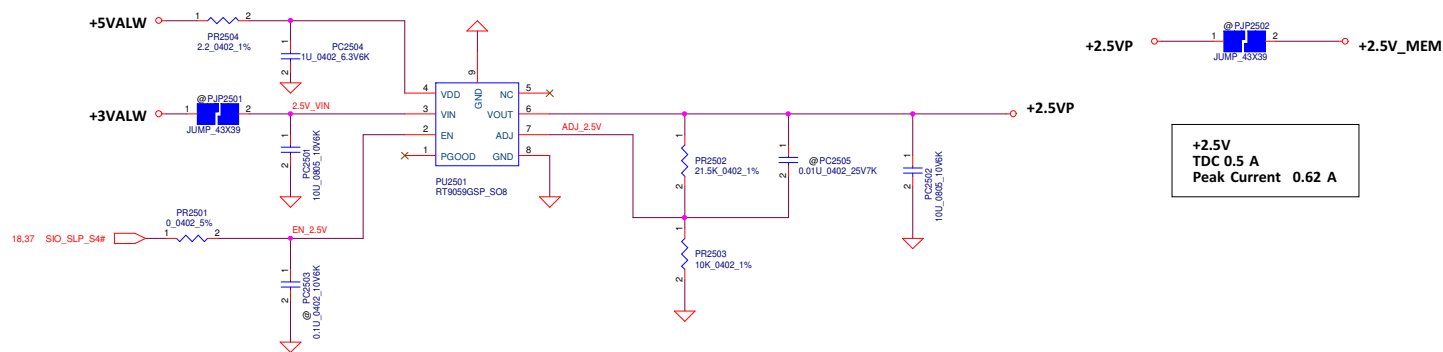
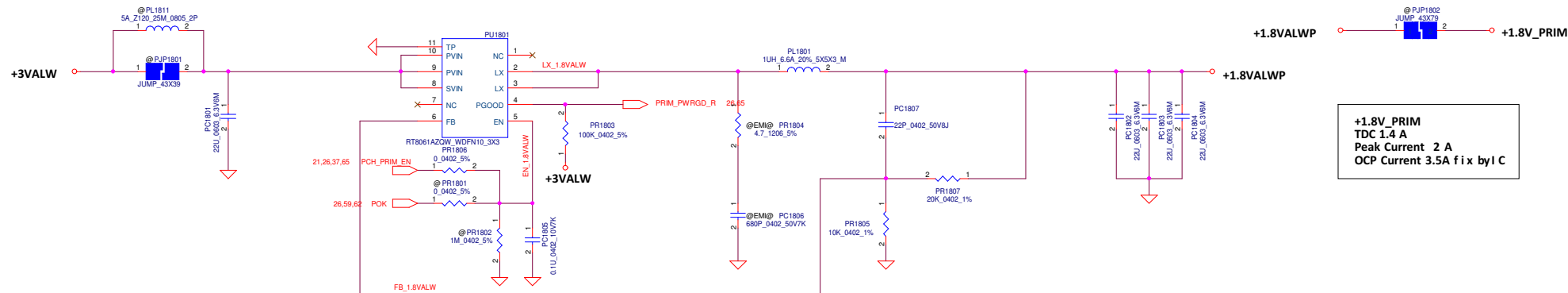
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				Size	Document Number	Rev
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Main Func = 1.05VALW



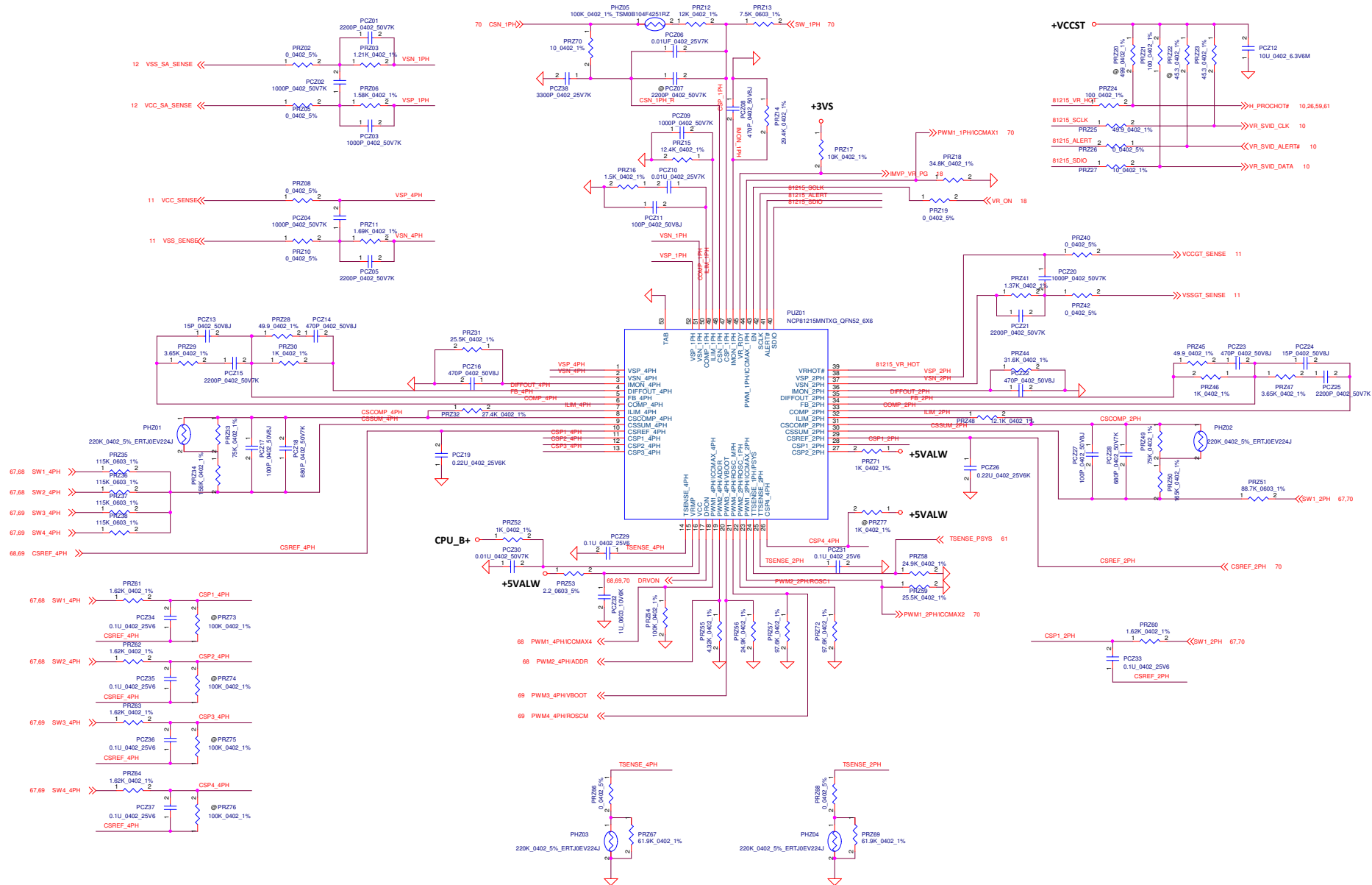
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Main Func = +1.8V_PRIM/+2.5V_MEM



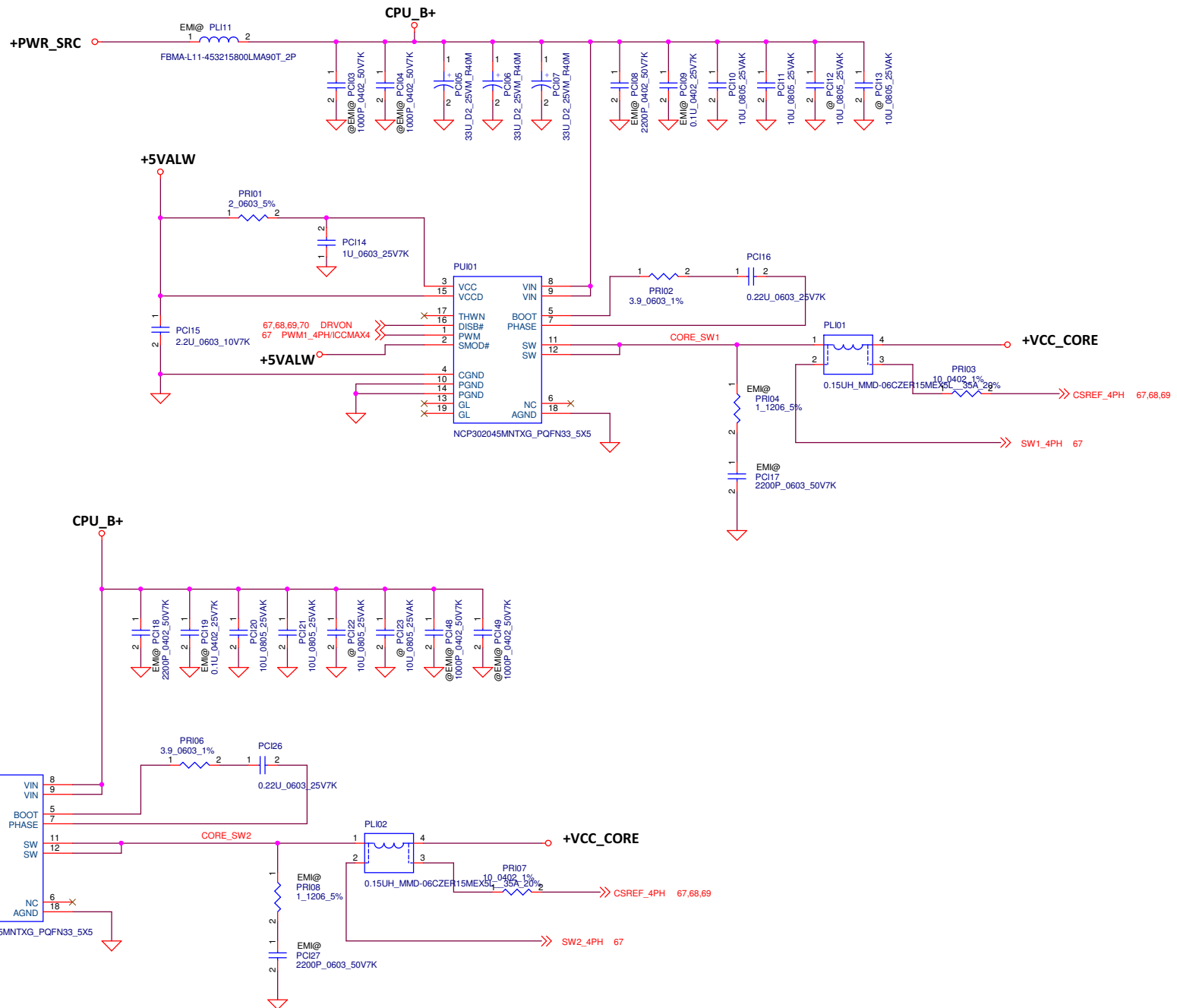
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Main Func = VCORE



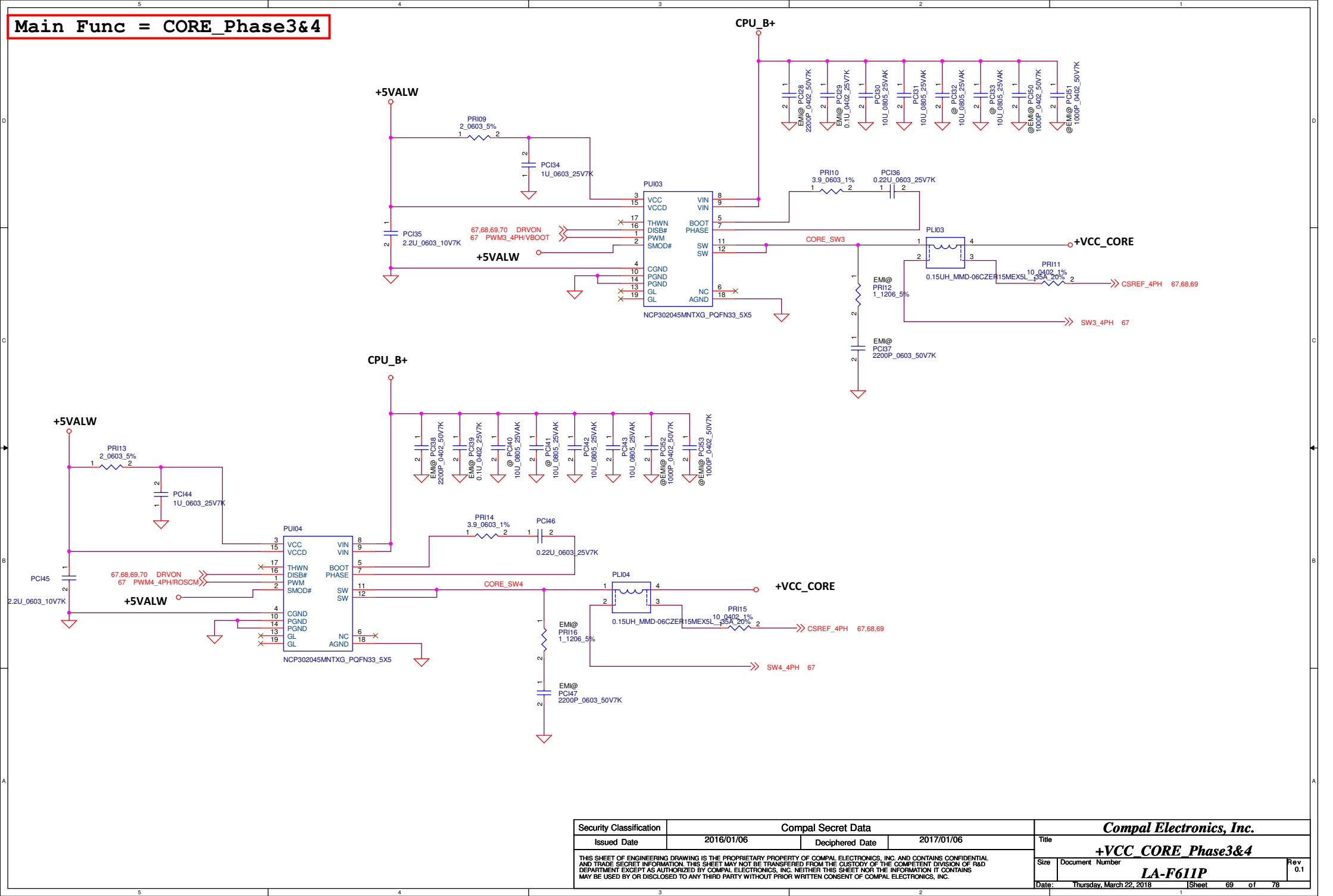
Main Func = CORE_Phase1&2

+VCC_CORE
TDC PL2 :80A
Peak Current 128A
OCP Current 154A
DCR 0.9mohm +/-5%
Load Line 1.8mV/A



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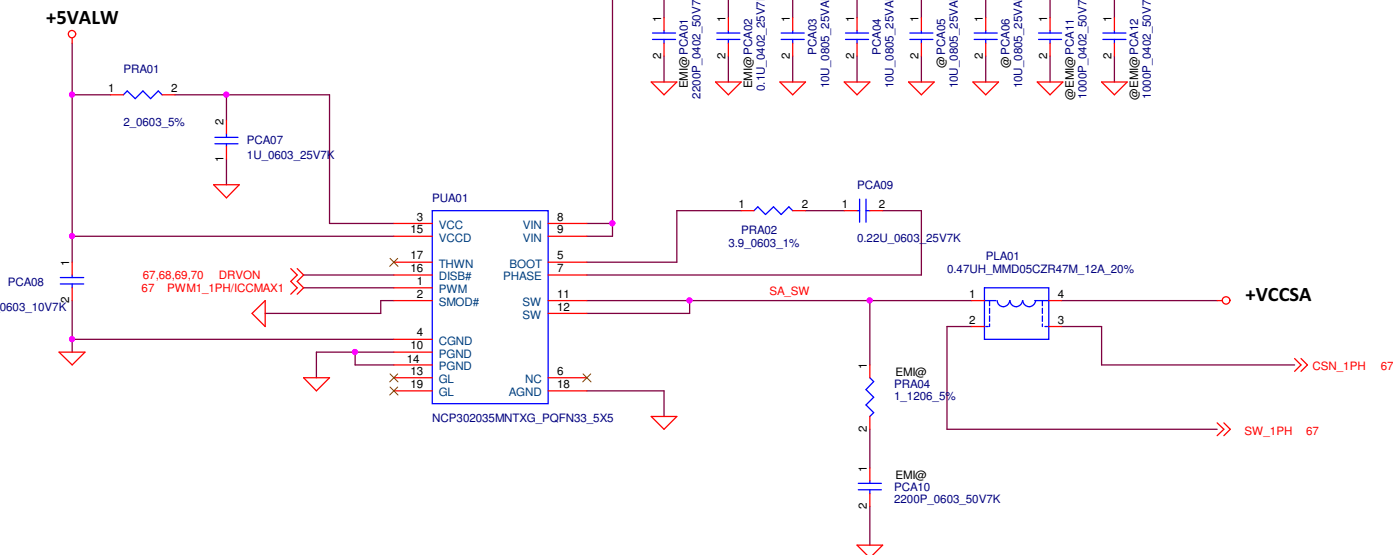
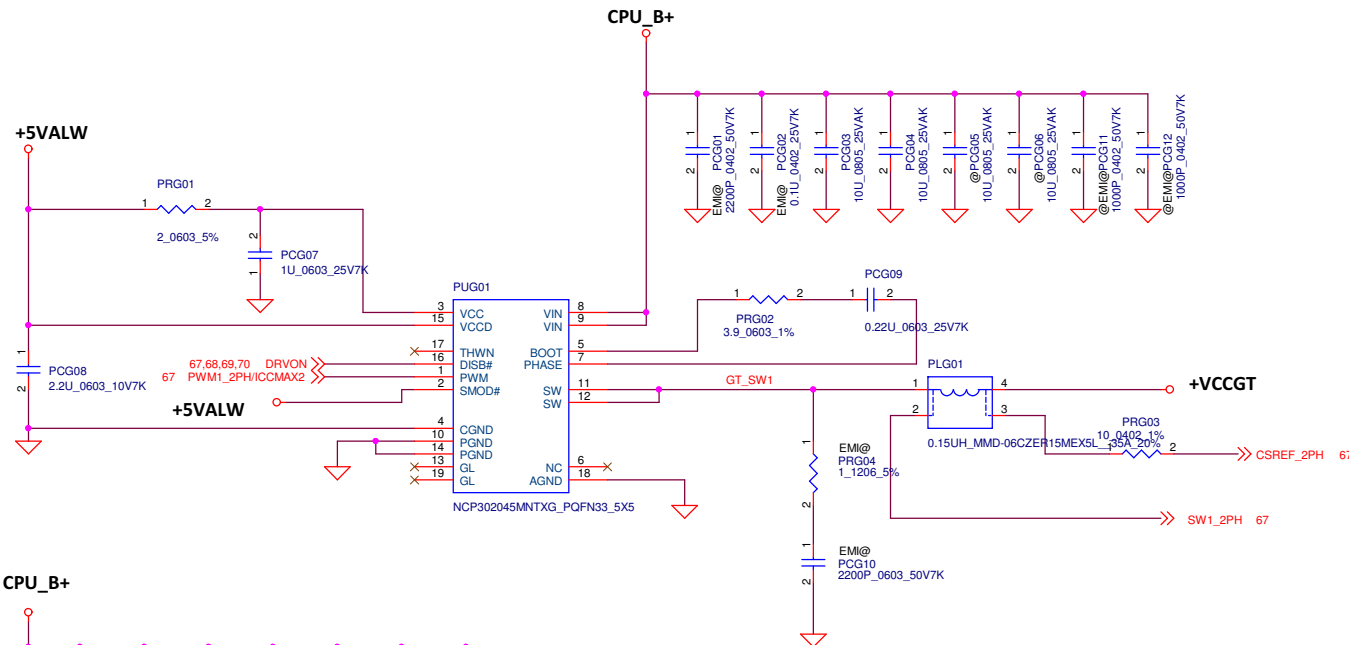
Main Func = CORE_Phase3&4



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Size		Document Number		Rev	
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Main Func = VCCGT/+VCCSA

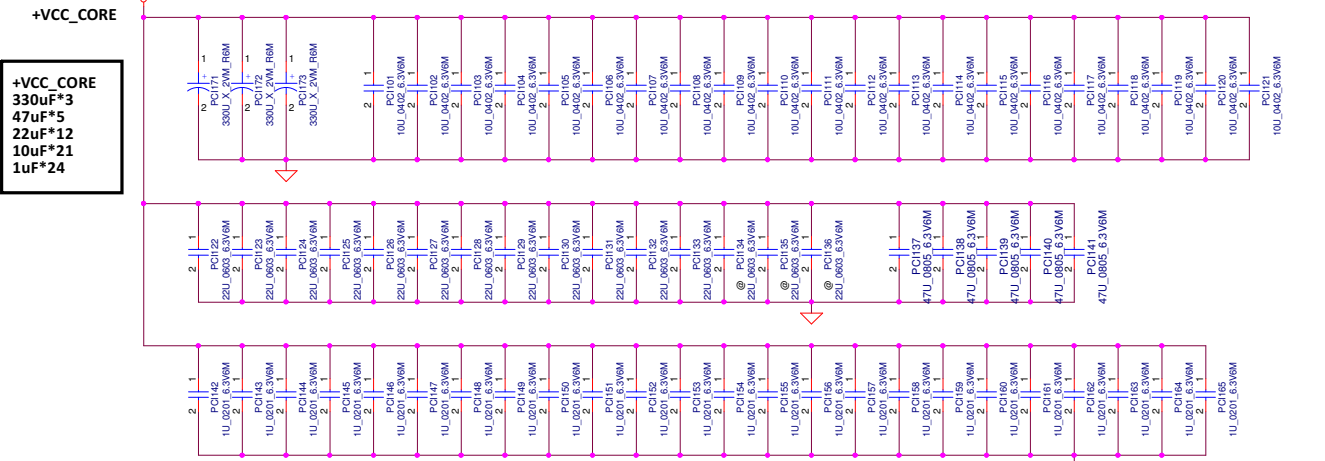
+VCCGT
TDC PL2 :25A
Peak Current 32A
OCP Current 39A
DCR 0.9mohm +/-5%
Load Line 2.7mV/A



+VCCSA
TDC PL2 :10A
Peak Current 11A
OCP Current 13A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A

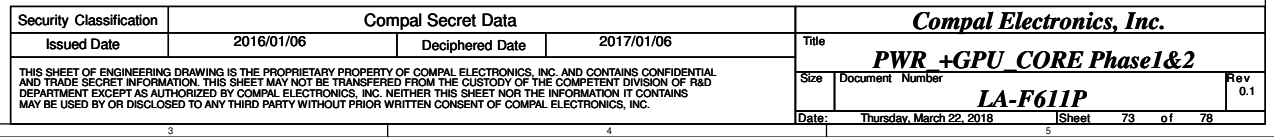
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Main Func = PWR_CPU DECOUPLING

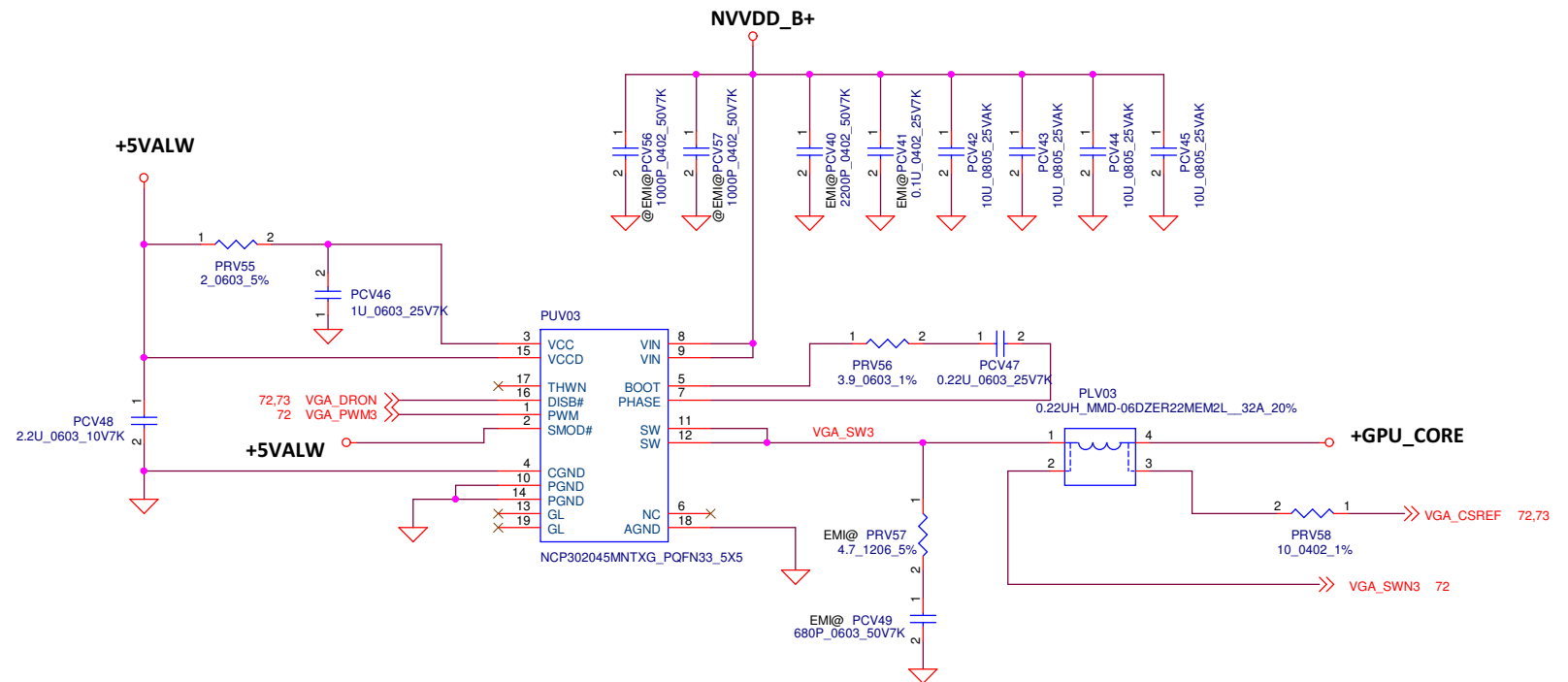


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+GPU_CORE
TDC 59A (46+13)
Peak Current 124A (106+18)
OCP=149A
Fsw=305KHz
DCR:0.98mohm +5%

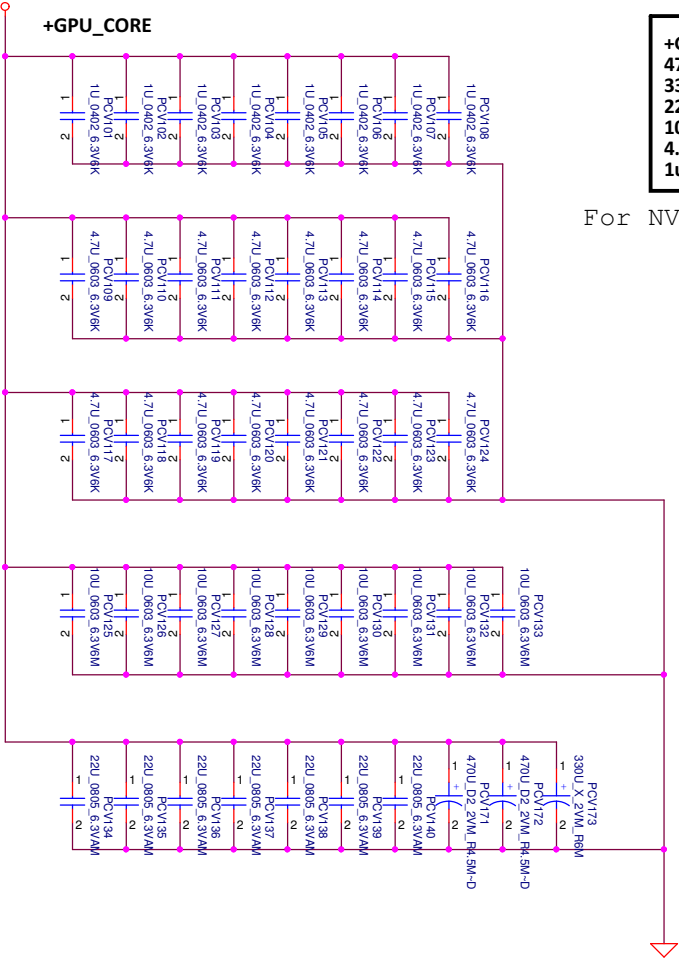


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Main Func = +GPU_CORE Phase3
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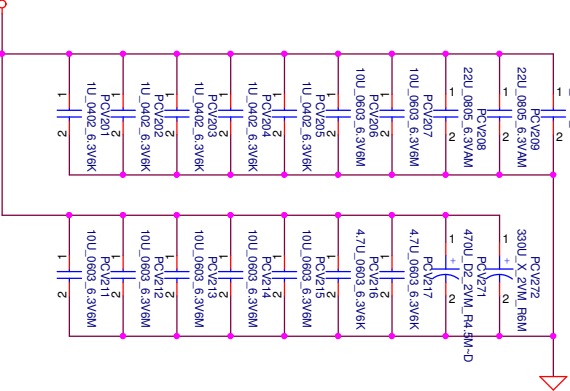
Main Func = VGA DECOUPLING



+GPU_CORE (NVVDD)
470uF X 2
330uF X 1
22uF_0805 X 7
10uF_0603 X 9
4.7uF_0603 X 16
1uF_0402 X 8

For NV N17P latest spec

+GPU_CORE

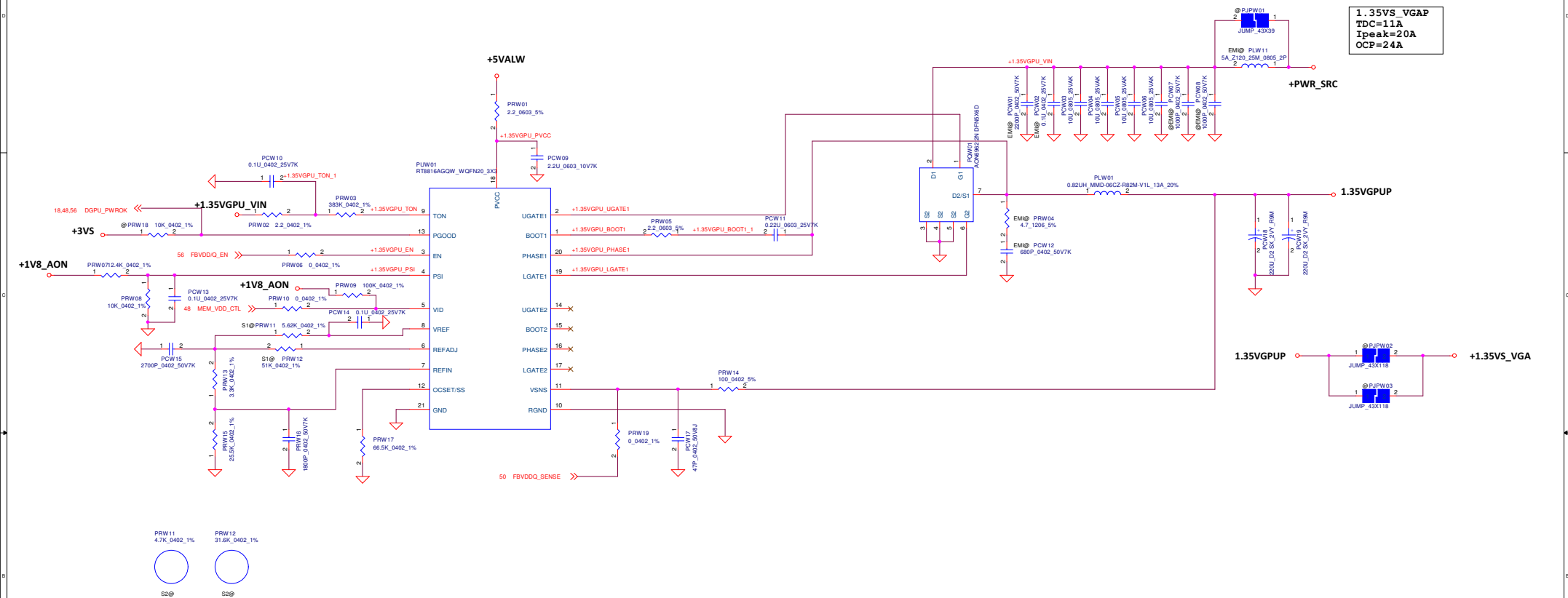


+GPU_CORE (NVVDD)
470uF X 1
330uF X 1
22uF_0805 X 3
10uF_0603 X 7
4.7uF_0603 X 2
1uF_0402 X 5

For NV N17P latest spec

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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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Main Func = +1.35VG PUP

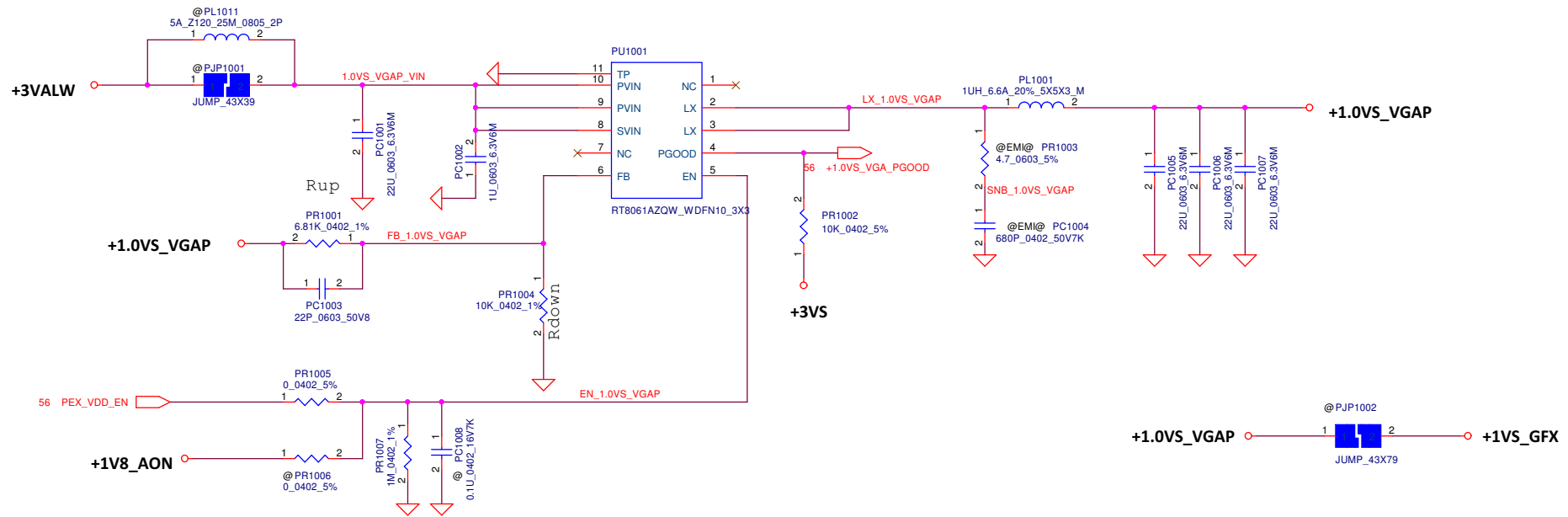


BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW11	PRW12
S1@ (4G)	N17P-G0/G1	256Mx32	Micron	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Hynix	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Samsung	1.35V & 1.5V	5.62K	51K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Hynix	1.35V & 1.55V	4.7K	31.6K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Samsung	1.35V & 1.55V	4.7K	31.6K

MEM_VDD_CTL	+MVDD
L	1.35V
H	1.5V/1.55V

Main Func = 1VS_GFX

+1VS_GFX
TDC 0.88A
Peak Current 1.1A
OCP current 4A



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